eRED-MOD

NETWORK AUDIO RENDERER

MODULE DATASHEET

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eRED-MOD-DS
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Preamble

I. About This Datasheet

This document provides the information required for integration and operation of the eRED-MOD Network Audio Renderer. For more information, please refer to the product description available from the engineered SA Web site at www.engineered.ch

II. Company Information

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It is important to operate this product within the specified input and output range described in this document. Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the product.

If you have questions regarding the input range, please contact engineered SA customer service prior to connecting the power supply. Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the product. Please consult the datasheet before connecting any load. If you have doubts concerning the load specification, please contact engineered SA customer service.

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Routine maintenance is not required. This product is warranted to be free of any defect with respect to performance, quality, reliability and workmanship for a period of SIX (6) months from the date of shipment from engineered SA.

In case it is proven that your product is actually defective during this warranty period only, engineered SA will gladly repair or replace this piece of equipment with a unit of equal performance characteristics.

Should this product be defective after expiration of your warranty period, engineered SA will repair this piece of equipment for as long as suitable replacement components are available. You, the owner, will bear any labor and/or component costs incurred in the repair or refurbishment of the said equipment, beyond the SIX (6) months warranty period. Any attempt to repair this product by anyone during this period other than by engineered or any authorised third party will void your warranty.

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VI. Documentation Release Notice

This document is under revision control and updates will only be issued as a replacement document with a new version number.

Product specifications are subject to change without notice.

1 Introduction

1.1 Highlights

The eRED-MOD module offers a top-notch solution for network audio playback systems. Developed exclusively for High-End systems, it allows for jitter-free, bit-perfect playback with no compromise on sound quality. Thanks to its compatibility with the UPnP AV 2.0 standards, its integration into a home network is easy. Key features for the eRED-MOD include:

- Digital Media Renderer for stereo audio
- UPnP AV 2.0 / DLNA
- Playing and decoding common audio formats* from HTTP streams
- 2-channel asynchronous endpoint for highest quality digital audio stereo playback
- Bit-perfect, jitter free data transmission
- PCM up to 32-bit resolution, sampling rate up to 384 kHz
- Support for DSD64, DSD128 and DSD256
- Support for gapless playback
- Ethernet interface
- I2S/DSD digital audio output
- Hardware mode for easy operation
- SPI interface available for extended features
- Single 3.3V power supply
- Compact design, low EMI

(*) Subject to licensing by the final product manufacturer for the various audio decoders.

The eRED-MOD module is a fully featured and easy-to-integrate OEM solution for network audio playback systems. Our proprietary concept for network audio playback takes care of the asynchronous mode, clock management, formats decoding and UPnP/DLNA support to provide an unprecedented listening experience. Latest high-resolution files, be they DSD or PCM, can be streamed from local or remote servers with perfect clocking and data integrity. This state-of-the-art concept is the solution for network connectivity, technically the best interface for digital music reproduction and a key component for any modern High-End DAC.

The eRED-MOD plays music from file servers or Internet streams, acting as a UPnP AV/DLNA Media Renderer device. Common PCM (Pulse Code Modulation) audio formats are supported, including decoding of lossless FLAC up to 384kHz. One-bit DSD (Direct Stream Digital) is also supported via uncompressed DSF and DFF files.

For optimal performances, Ethernet streaming is based on an asynchronous protocol. Thus, the digital audio output port of the eRED-MOD is synchronized by the external clock and assures jitter-free clocking. Master and slave modes are offered on the I2S port.

1.2 eRED-MOD Block Diagram

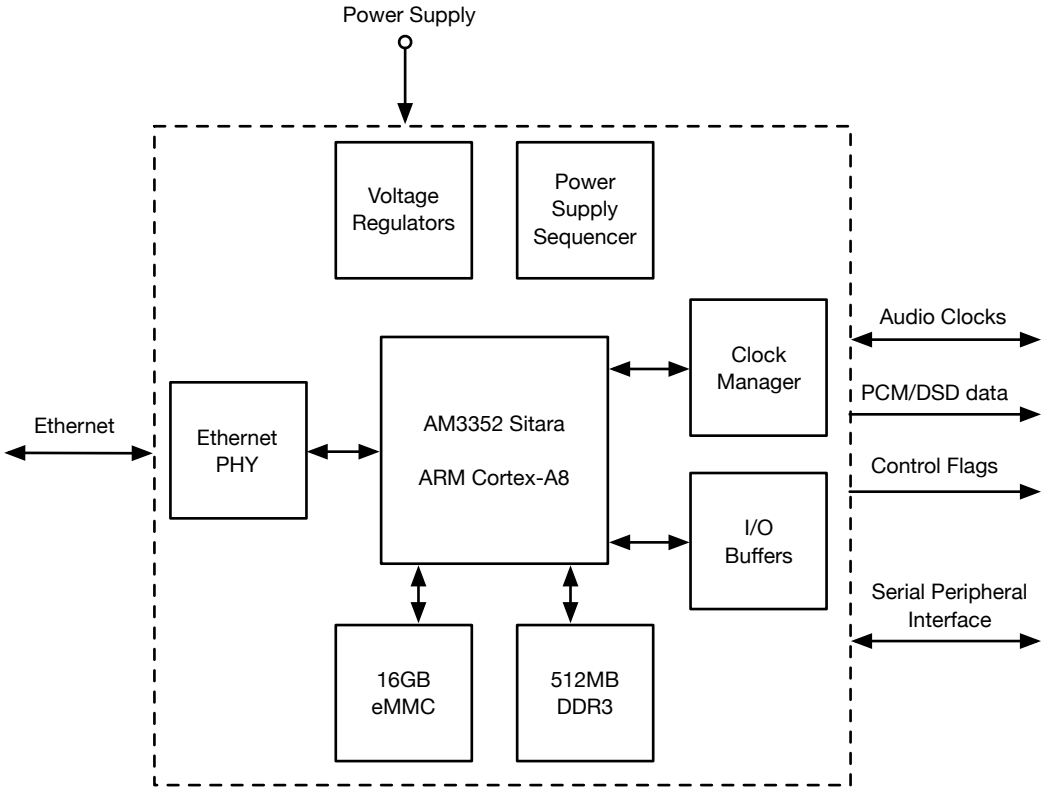

Figure 1-1 – eRED-MOD simplified block diagram

Refer to chapter 4 for more details about eRED-MOD integration, as well as general information relative to network audio systems.

3 Characteristics and Specifications

3.1 Electrostatic Discharge Warning

Many of the components in this product are subject to be damaged by electrostatic discharge (ESD). Customers are advised to observe proper ESD precautions when unpacking and handling the board, including the use of a grounded wrist strap at an approved ESD workstation.

Caution: Failure to observe ESD handling procedures may result in damage to the product.

3.2 Recommended Operating Conditions

Table 3-1 indicates the recommended conditions under which the product should run properly.

Parameter	Recommend Condition
Power supply voltage	3.30 VDC
Operating free-air temperature	$T_{A(min/max)}$: 0 °C / 60 °C

Table 3-1 – Recommended operating conditions

3.3 Absolute Maximum Ratings

The user should be aware of the absolute maximum operating conditions for the eRED-MOD. Failure to comply with these conditions may result in damage to the product. The minimum and maximum values are indicated in Table 3-2.

Parameter	Min.	Max.
Power supply voltage	-0.30 V	3.60 V
Input signal voltage	-0.30 V	3.60 V

Table 3-2 – Absolute maximum ratings

3.4 Electrical Specifications

Parameter	Min.	Typ.	Max.	Unit
External DC supply voltage	3.15	3.30	3.45	V
External DC supply current		250	350	mA
CMOS output high level V_{IH}	2.7	3.10	3.30	V
CMOS output low level V_{IL}	0	0.20	0.40	V

Table 3-3 – Electrical specifications

3.5 Audio Resolution Specification

Parameter	Min.	Typ.	Max.	Unit
PCM digital audio resolution	16		32	bit
PCM digital audio sample rate	32		384	kHz
PCM digital audio dynamic range		32		bit
DSD sample rate	2.8224		11.2896	MHz

Table 3-4 – Audio resolution specifications

3.6 Pin Configuration

The eRED-MOD uses Hirose FX8-60P-SV connectors on PCB's bottom side. For physical location of the pins, refer to chapter 6.

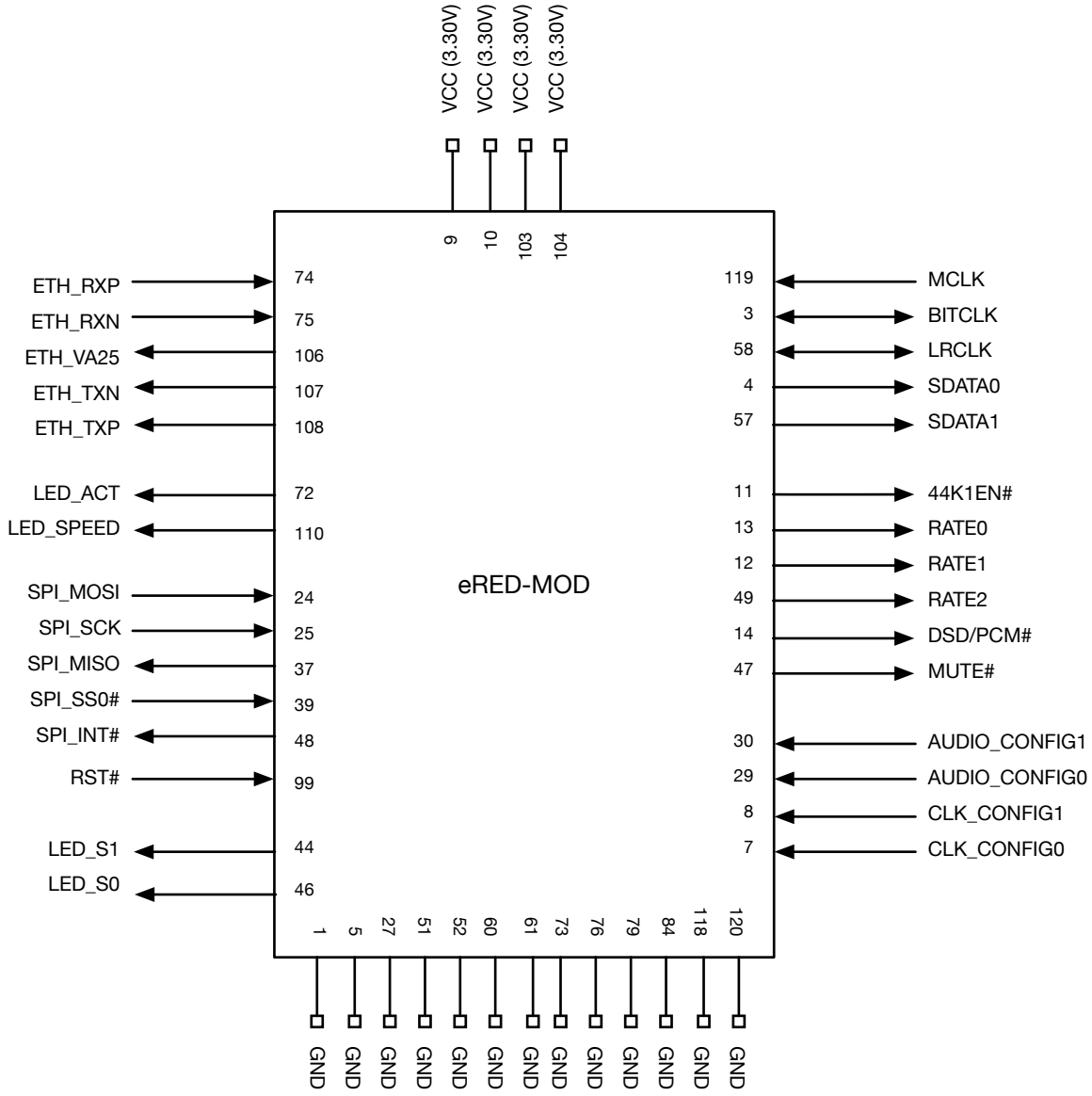

Figure 3-1– eRED-MOD pin configuration

3.7 Pin Functions

Pin assignments are described in the table hereafter. Items not listed here are reserved for factory use and must be left unconnected.

Pin #	Name	Type	Description
1	GND	Power	Ground
3	I2S_BITCLK	Input/output	I2S input/output port BITCLK Serial bit clock for audio data
4	I2S_SDATA0	Output	I2S output port SDATA0 Stereo PCM audio data or DSD left-channel audio data
5	GND	Power	Ground
7	CLK_CONFIG0	Input	audio clock config (1) - unused yet, leave open
8	CLK_CONFIG1	Input	audio clock config (1)
9	VCC (3.3V)	Power	Power supply, 3.30V
10	VCC (3.3V)	Power	Power supply, 3.30V
11	CC_44K1EN#	Output	Audio sampling rate information flag low for 44.1kHz-based sampling rate, high for 48kHz-based sampling rate
12	CC_RATE1	Output	Audio sampling rate information flag
13	CC_RATE0	Output	Audio sampling rate information flag
14	CC_DSD/PCM#	Output	Audio data type information flag low for PCB, high for DSD
24	SPI_MOSI	Input	Slave SPI data input (1)
25	SPI_SCK	Input	Slave SPI serial clock (1)
27	GND	Power	Ground
29	AUDIO_CONFIG0	Input	Audio processing config (1) - reserved for future use, leave open
30	AUDIO_CONFIG1	Input	Audio processing config (1) - reserved for future use, leave open
37	SPI_MISO	Output	Slave SPI data output
39	SPI_SS0#	Input	Slave SPI chip select (1), active low
44	LED_S1	Output	System status LED, active high
46	LED_S0	Output	System status LED, active high
47	CC_MUTE#	Output	Audio MUTE signal, active low
48	SPI_INT#	Output	Slave SPI open collector, active low
49	CC_RATE2	Output	Audio sampling rate information
51	GND	Power	Ground
52	GND	Power	Ground
57	I2S_SDATA1	Output	I2S output port SDATA1 DSD right-channel audio data
58	I2S_LRCLK	Output	I2S output port LRCLK Frame sync clock for PCM audio data
60	GND	Power	Ground
61	GND	Power	Ground
72	ETH_LED_ACT	Output	Ethernet PHY LED1 – blink on LAN activity, active low
73	GND	Power	Ground

Pin #	Name	Type	Description
74	ETH_RXP	Input/output	Ethernet PHY RXP
75	ETH_RXN	Input/output	Ethernet PHY RXN
76	GND	Power	Ground
79	GND	Power	Ground
84	GND	Power	Ground
99	RST#	Input	Master reset (1), active low
103	VCC (3.3V)	Power	Power supply, 3.30V
104	VCC (3.3V)	Power	Power supply, 3.30V
106	ETH_VA25	Power	Ethernet PHY voltage reference
107	ETH_TXN	Input/output	Ethernet PHY TXN
108	ETH_TXP	Input/output	Ethernet PHY TXP
110	ETH_LED_SPEED	Output	Ethernet PHY LED2 - indicates LAN speed low for 100Mb, high for 1Mb
118	GND	Power	Ground
119	MCLK	Input	Master clock input for I2S output port (1), Clock Master Mode only
120	GND	Power	Ground

Table 3-5 – Pin functions

(1) This pin has an internal weak pull-up.

4 Application Information

4.1 Typical Network Audio Setup

A network audio setup is typically composed of the following devices:

- Digital Media Server (DMS) – Multimedia files are stored on this device and are made available to the network.
- Digital Media Renderer (DMR) – This device is the rendering output, able to play content from a Media Server and controlled by a Digital Control Point.
- Digital Control Point (DCP) – This device browses the content provided by Media Servers and sends commands to the Media Renderer for rendering the selected media.

Playback starts once the Control Point has sent a file path and "play" command to the Media Renderer. The Media Renderer fetches the file directly from the Media Server, and the data stream does not pass through the Control Point.

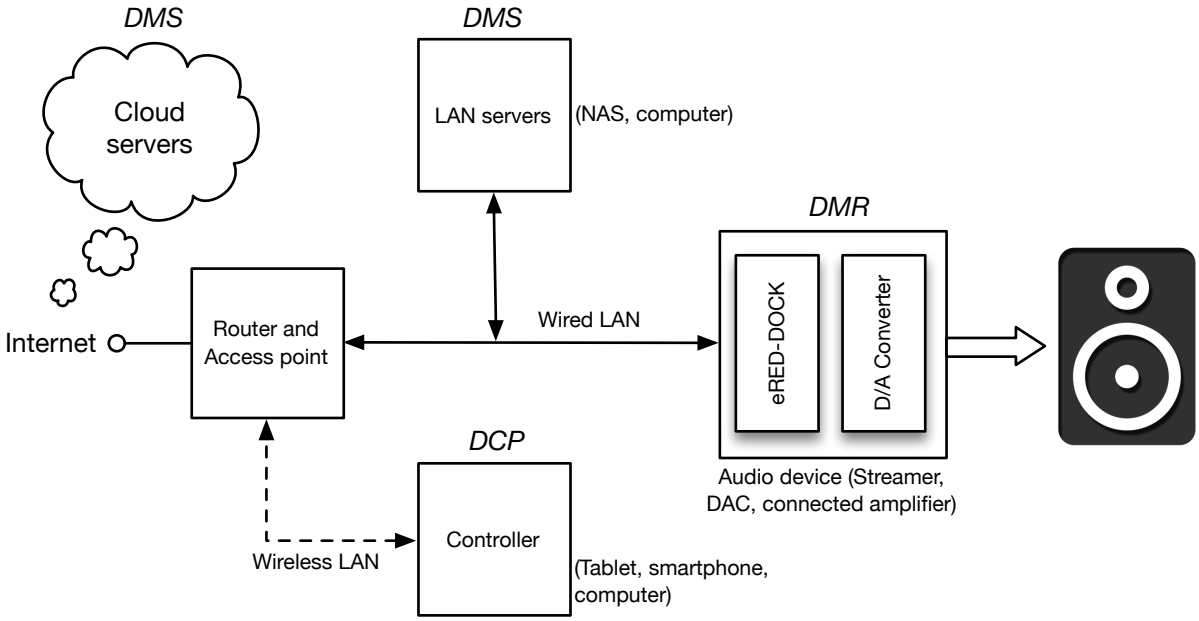

Figure 4-1 - Typical Network Audio Setup

4.2 Audio Formats

The design supports both multi-bit PCM and one-bit DSD (Direct Stream Digital) modulations.

The following stereo audio formats are supported and decoded by the eRED-MOD interface:

- FLAC (Free Lossless Audio Codec)
- WAV (Waveform Audio File Format)
- MP3 (Mpeg Audio Layer 3)
- ALAC (Apple Lossless Audio Codec)
- AAC (Advanced Audio Coding)
- AIFF (Audio Interchange File Format)
- Uncompressed DSF and DFF (DSD stream file)

Standard WAV and AIFF files contain uncompressed pulse-code modulation (PCM) audio data. Like any non-compressed, lossless format, they use much more disk space than compressed formats. Such uncompressed PCM streams are supported up to 384 kHz / 32-bit.

FLAC is an open format with royalty-free licensing. It supports for metadata tagging, album cover art, and fast seeking. The technical strength of FLAC compared to other lossless formats lies in its ability to be streamed and decoded quickly, independently of the compression level. Since FLAC is a lossless scheme, it is suitable as an archive format for CDs and other media owners who wish to preserve their audio collections. The eRED-MOD decodes FLAC files up to a sampling rate of 384kHz.

MP3 and AAC are lossy compressions and encoding schemes for digital audio. These are non-free codecs covered by patents and subject to licensing by the final product manufacturer. The eRED-MOD offers the technical ability to decode such formats, but engineered SA is not responsible for non-free audio codecs licensing.

DSF and DFF files may contain multi-channel audio data and various resolutions. The eRED-MOD supports uncompressed one-bit stereo audio at 2.8224 MHz, 5.6448 MHz and 11.2896 MHz

Note: It is the responsibility of the manufacturer of the final product (the brand) to take care of the licensing and fees for the non-free audio codecs.

4.3 Typical Application

Applications include all types of audio streaming devices, like D/A converters and network bridges. Typically, the digital audio output bus or the eRED-MOD is connected to:

- a Digital to Analog converter (DAC)
- a Digital Audio Transmitter (DIT) in order to output S/PDIF signal
- a DSP to apply digital processing (e.g. oversampling)
- an FPGA for clock and signal routing

Figure 4-2 illustrates a possible eRED-MOD integration within a complete system with D/A conversion for analog outputs as well as digital S/PDIF output where low level management is performed by a local micro-controller (MCU).

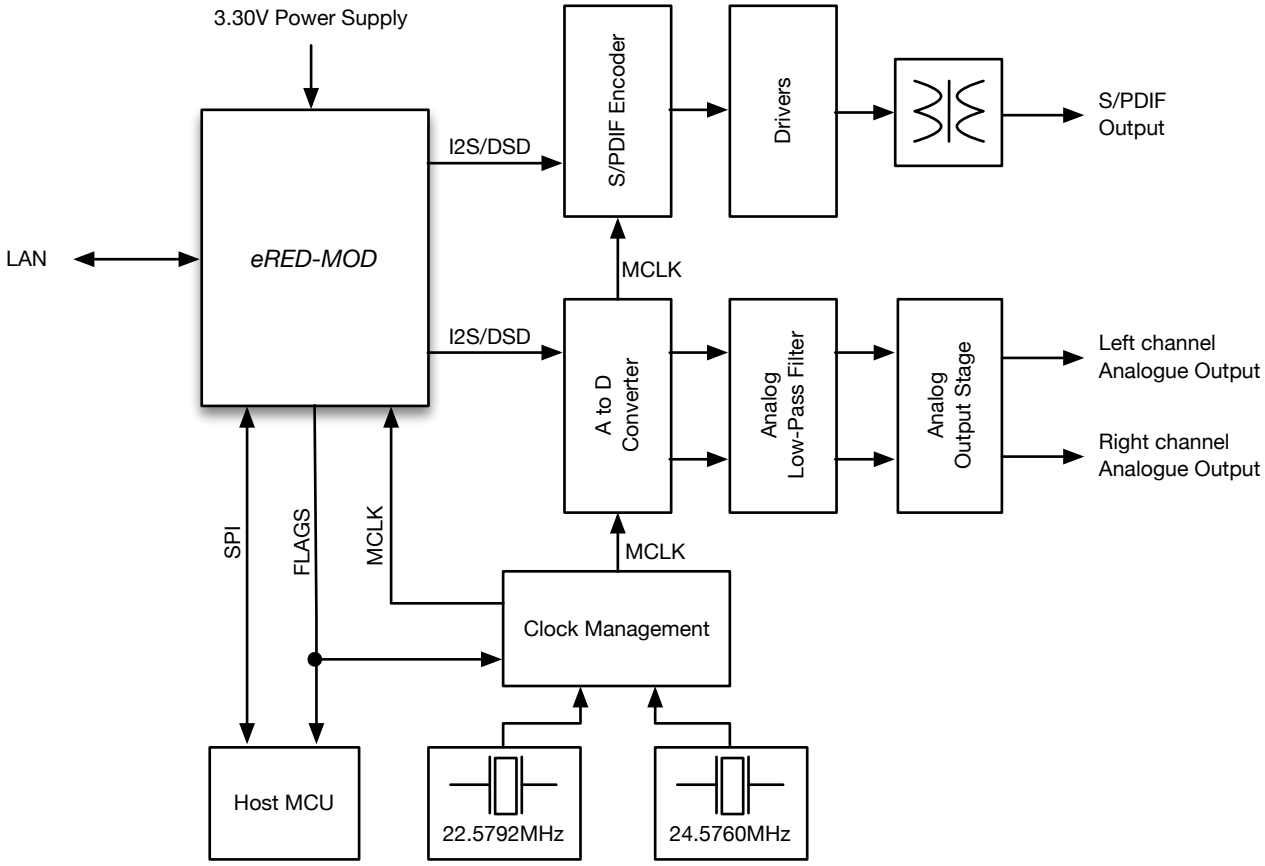

Figure 4-2 – Typical eRED-MOD integration

4.4 Power Supply recommendation

The eRED-MOD operates from a single 3.30V supply. It integrates a voltage supervisor that resets the system when the power supply drops below a defined threshold. Power supply regulation, voltage precision, current capability and connection impedance are important factors to ensure clean operation.

For optimal operation of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR 0.1 µF and 10 µF X7R ceramic decoupling capacitors close to each supply pin, placed as close to the device as possible. The bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources to the circuitry.
- Module ground pins have to be connected to a low-impedance system reference point, such as the system digital ground plane.

Caution: Failure to respect the power supply polarity and voltage level may result in damage to the product.

4.5 Clock Management

The eRED-MOD implements a sophisticated asynchronous network data transfer with a large buffer in order to avoid jitter and get the highest digital audio playback quality. Thus, the digital audio output bus is driven only by the local clocks.

The I2S output port of the module can be configured as Clock Master or Clock Slave device. This offers flexibility with regards to the host circuitry but has no direct impact on the asynchronous transfer and jitter-free concept. Master or Slave mode is chosen by setting CLK_CONFIG1 as indicated in Table 4-1.

CLK_CONFIG1	LRCLK / BITCLK mode	LRCLK / BITCLK type	MCLK type
Low	Master Mode LRCLK and BITCLK are supplied to the host	Output	Input
High	Slave Mode LRCLK and BITCLK are supplied by the host	Input	Unused – leave unconnected

Table 4-1 – Clock configuration

In Slave Mode BITCLK and LRCLK have to be supplied by an external device, being a D/A converter, an FPGA or any other circuit able to be Clock Master on the digital audio bus.

However, BITCLK and LRCLK frequency have to match the sampling rate of the track being played over the network according to the hardware flags CC_RATE0, CC_RATE1 and CC_RATE0. Refer to Table 4-2 and Table 4-3. In this situation, MCLK Input is discarded.

When using the eRED-MOD in Master Mode, only MCLK has to be supplied. BITCLK and LRCLK are automatically generated by the eRED-MOD according to the current sampling rate. Therefore, the host has only to supply the appropriate MCLK frequency according to the hardware flag 44K1EN#, as described in Table 4-3.

4.6 I2S Digital Audio Bus

The digital audio port is configured in standard I2S. The data signals are made of two lines: SDATA0 and SDATA1. By default, only SDATA0 is used in PCM audio.

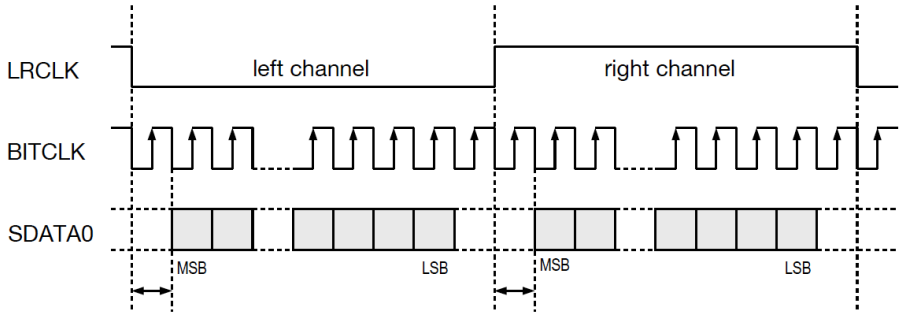

Figure 4-3– I2S data format

Clock management information is made of four signals: RATE0, RATE1, RATE2 and 44K1_EN#. Please note that RATE2 is unused yet and reserved for future upgrades. These flags reflect the sampling frequency of the audio source track currently playing and media server configuration.

LRCLK Frequency	RATE0	RATE1	44K1_EN#
44.1 kHz	High	High	Low
48 kHz	High	High	High
88.2 kHz	Low	High	Low
96 kHz	Low	High	High
176.4 kHz	High	Low	Low
192 kHz	High	Low	High
352.8 kHz	Low	Low	Low
384 kHz	Low	Low	High

Table 4-2 – Relation between sampling frequency and hardware flags

Table 4-3 shows how the audio sampling frequency (LRCLK), the bit clock (BITCLK) frequency and the master clock (MCLK) frequency are related.

LRCLK Frequency	BITCLK Ratio	MCLK Ratio	MCLK Frequency
44.1kHz	64 * Fs	512 * Fs	22.5792MHz
48kHz	64 * Fs	512 * Fs	24.5760MHz
88.2kHz	64 * Fs	256 * Fs	22.5792MHz
96kHz	64 * Fs	256 * Fs	24.5760MHz
176.4kHz	64 * Fs	128 * Fs	22.5792MHz
192kHz	64 * Fs	128 * Fs	24.5760MHz
352.8kHz	64 * Fs	64 * Fs	22.5792MHz
384kHz	64 * Fs	64 * Fs	24.5760MHz

Table 4-3 – relation between left/right clock, master clock and bit clock

4.7 DSD Mode

In DSD mode, I2S_SDATA0 outputs left-channel DSD data and I2S_SDATA1 outputs right-channel DSD data. I2S_LRCLK must be discarded.

Pin #	Name	PCM Signal	DSD Signal
3	I2S_BITCLK	BITCLK	BITCLK
58	I2S_LRCLK	LRCLK	discarded
4	I2S_SDATA0	PCM data L/R	DSD data left
57	I2S_SDATA1	n/a	DSD data right
14	CC_DSD/PCM	Low	High

Table 4-4 – pin mapping in PCM and DSD mode

Support for native DSD64, DSD128 as well as DSD256 is provided by the MR-MOD module. DSD data format is indicated by the flag CC_DSD/PCM on pin 14.

CC_DSD/PCM	Data Stream Type
Low	PCM
High	DSD

Table 4-5 – Data stream type

Table 4-6 shows how the DSD frequency is indicated by the hardware flags, and Table 4-7 illustrates the relation between DSD rate, Bit Clock and Master Clock frequencies.

DSD Type	RATE0	RATE1	44K1_EN#
DSD 64	High	High	Low
DSD 128	Low	High	Low
DSD 256	Low	Low	Low

Table 4-6 – Relation between DSD rate and hardware flags

DSD Type	Bit Clock Frequency	Master Clock Frequency
DSD 64	2.8224MHz	22.5792MHz
DSD 128	5.6448MHz	22.5792MHz
DSD 256	11.2896MHz	22.5792MHz

Table 4-7 – Relation between DSD rate, bit clock and master clock

4.8 MUTE# signal

The MUTE# (active low) signal indicates that the serial data are no longer valid and therefore should be discarded. In order to avoid switching noise, the DAC shall be muted according to the MUTE# signal and during sampling rate or data format change.

4.9 Ethernet Interfacing

The eRED-MOD integrates an on-board Ethernet interface. Only the RJ45 connector and ESD protection are needed on the backplane board, as shown on the circuit diagram here below.

Using an RJ45 connector jack with integrated magnetics is highly recommended. The magnetics protect against faults and transients, including rejection of common mode signals between the transceiver and the cable. These signals are commonly caused by electromagnetic interference (EMI), either from noise picked up by the cable or from slight impedance mismatches. The magnetics also provide galvanic isolation from Ethernet cables, and offset any DC biasing caused by connected nodes having been powered from different sources.

For optimal operation of the device, use good printed circuit board (PCB) layout practices, including short traces and impedance control according to Ethernet / LAN specifications.

Note: RJ45 connector shown here is based on part number J0011D01NL from Pulse Electronics Corporation for reference only. Pin numbering varies from one manufacturer/model to the other.

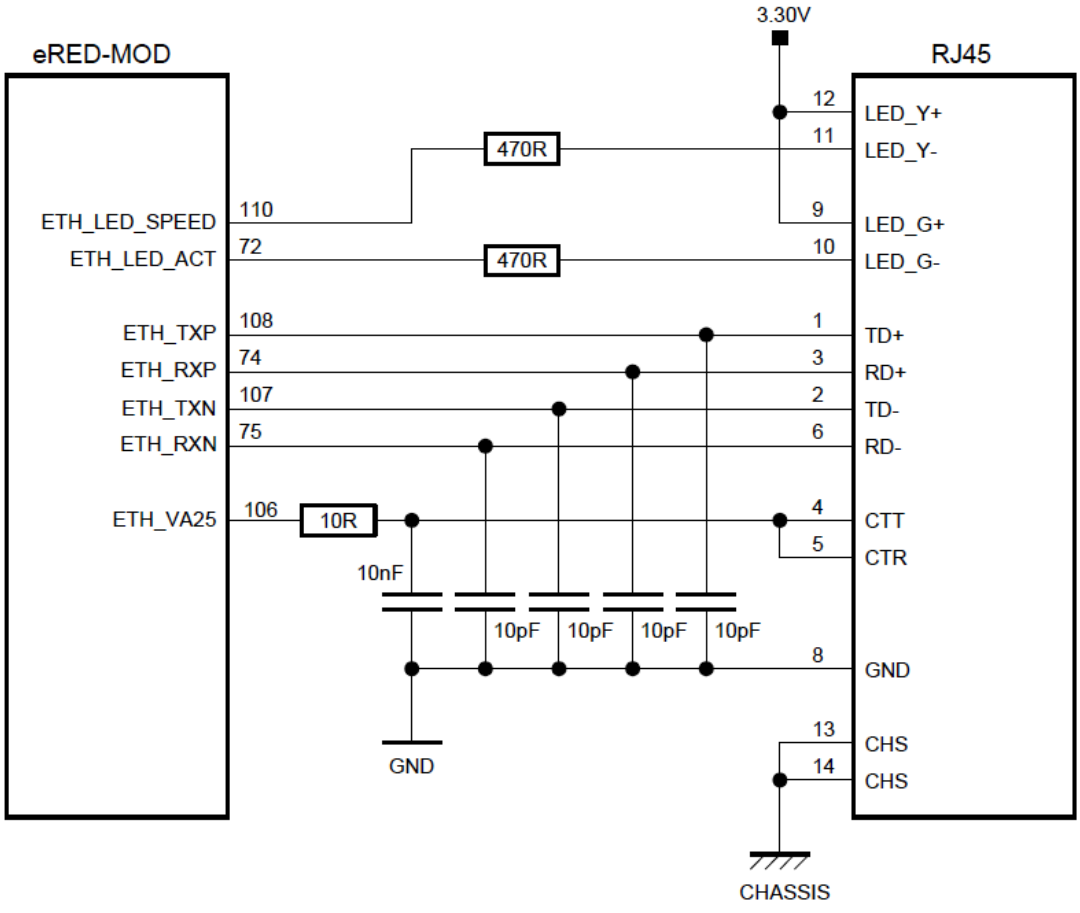

Figure 4-4 – Ethernet interfacing

4.10 Network Connection

The eRED-MOD is compatible with the UPnP AV/DLNA specification and no specific user configuration is required to integrate it into an Ethernet network. There must be a DHCP server on the network where the eRED-MOD operates so that it can fetch its IP address.

Basic boot status is provided by two signals, as indicated in the table below. These signals can be directly connected to status LEDs for diagnostic.

LED_S1	LED_S0	Description
1	1	Power up, booting
1	0	System booted, waiting for DHCP server
0	1	System booted and network configured, ready to operate
0	0	System Idle

Table 4-8 – status LED description

4.11 Configuration web page

Accessing the eRED-MOD configuration web page requires a computer or any device with a web browser connected on the same network. The last digits of the renderer's IP address are indicated at the end of its UPnP *friendly name*. This allows to access the web page by introducing its IP address into a web browser, but most of the UPNP control apps offer a direct link to the page.

The eRED-MOD configuration web page provides an interface for Firmware Update and customizing the renderer's UPnP *friendly name*.

5 Serial Peripheral Interface

5.1 Interface description

The eRED-MOD interface features a full-duplex serial port based on the Serial Peripheral Interface standard.

The SPI port communicates in slave mode. It is used to access registers allowing the eRED-MOD to transmit information to the host device, referred as master, and to be configured for the desired operational mode.

The SPI port is a five-wire serial interface where SPI_CS# (active low) is the module chip select signal, SPI_SCK is the control port serial clock from the master device, SPI_MOSI is the input data line from master, SPI_MISO is the output data line to the master and SPI_INT is the interrupt line.

Data words are 16-bit long and transmitted in MSBF format. Data is clocked in on the rising edge of SPI_SCK and clocked out on the falling edge. Figure 5-1 and Figure 5-2 illustrate the operation of the SPI port as well as the protocol for register read and write operations.

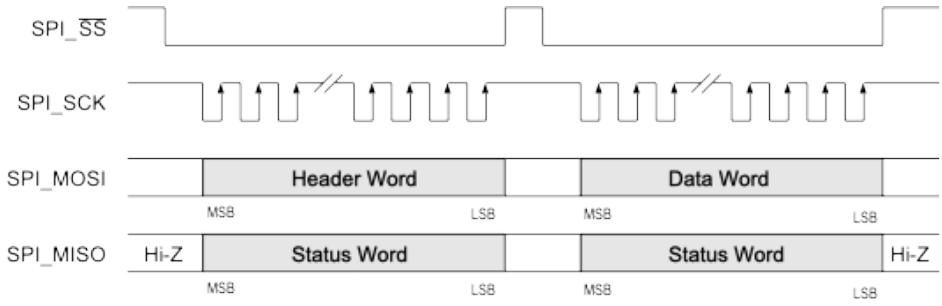

Figure 5-1 - SPI sequence for register WRITE

The register WRITE operation requires two 16-bit words to be sent by the host device. A handshaking mechanism ensures that the transfer is valid. Refer to the register description hereafter for detailed information.

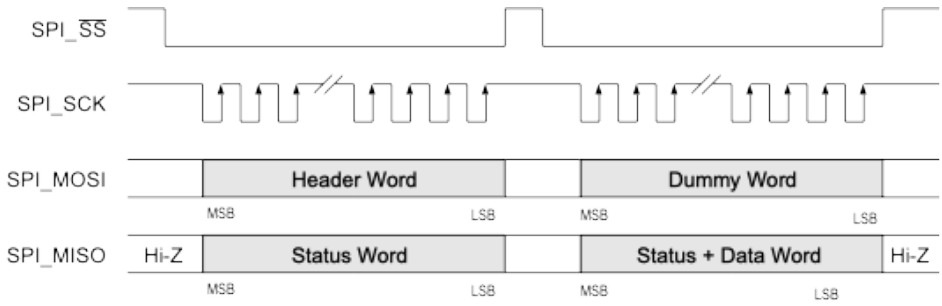

Figure 5-2 - SPI sequence for register READ

The register READ operation requires two 16-bit words to be sent by the host device, the second one being a dummy word. A handshaking mechanism ensures that the transfer is valid. Refer to the register description hereafter for detailed information.

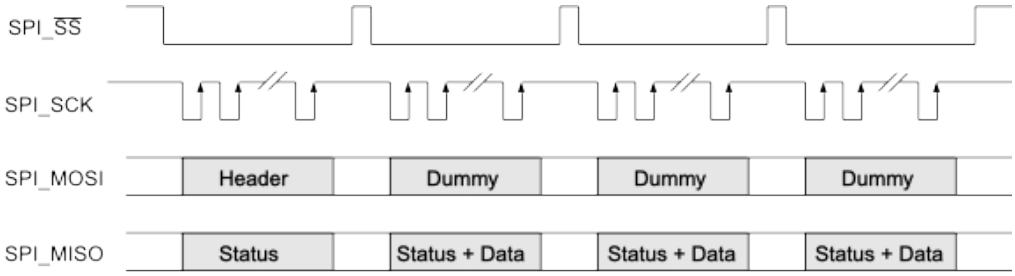

Figure 5-3 - SPI sequence for register BURST READ

Some registers allow reading more than one word and therefore a longer data transfer is required. This happens with STRING data types. When accessing these registers, a BURST READ transfer is used. The length of the transfer depends on the data type.

A register access is made of one HEADER word followed by one or more DATA/DUMMY word. Delay between each word transferred is critical, please refer to the timing specification given in chapter 5.4. If the maximum delay is not respected, a timeout occurs, the communication is reset, and the next expected word is a HEADER.

All transfers rely upon a handshaking mechanism. This handshaking mechanism uses four bits of the word transmitted by the eRED-MOD to the host. The VALID bit indicates whenever the SPI transfer is valid or not, meanwhile the PARITY bit allows for parity check. The READY bit indicates if the device is ready to process the transfer or if this must be repeated. The STATE bit indicates if the current transfer is related to a HEADER or a DATA word.

READY bit cleared means that the eRED-MOD is not ready to process the communication. The last word sent by the host is lost, and the reply is not valid. The last word must be sent again by the host until READY is set. A wrong VALID or PARITY bit means a transmission error occurred. The use must abort the transfer and wait at least the communication timeout before restarting a new transfer. The STATE bit is here to help the user to detect a misalignment in the HEADER/DATA sequencing. Handling of this bit is not mandatory.

The HEADER word sent by the host is defined as follows:

Word name	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
HEADER	0	0	0	0	0	0	0	0	R/W	A6	A5	A4	A3	A2	A1	A0

Figure 5-4 - HEADER word definition

Bit 15-8 : Set to 0
Bit 7 : R/W, defines a READ or WRITE sequence
0 = WRITE sequence
1 = READ sequence
Bit 6-0 : A6-A0, register address

The DUMMY word sent by the host for a register READ sequence is not used. All bits must be set to zero. The Data Word sent by the host for a register WRITE operation is defined as follows:

Word name	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
DATA	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

Figure 5-5 - DATA word definition

Bit 15-8 : Set to 0
Bit 7-0 : DATA

The STATUS word provided by the eRED-MOD is defined as follows:

Word name	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
STATUS	READY	STATE	PARITY	VALID	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 - STATUS word definition

MSB : READY
0 = device is not ready and transfer failed
1 = device is ready and transfer succeeded
Bit 14 : STATE, indicates whenever the word received by the eRED-MOD is a HEADER or a DATA
0 = DATA
1 = HEADER
Bit 13 : PARITY, even parity in bits 15 to 0
Bit 12 : VALID
0 = transfer succeeded
1 = transfer failed
Bit 11-0 : Set to 0

The STATUS + DATA word provided by the eRED-MOD

Word name	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
STATUS+DATA	READY	STATE	PARITY	VALID	0	0	0	0	D0	D6	D5	D4	D3	D2	D1	D0

Figure 5-7 – STATUS + DATA word definition

MSB : READY
0 = device is not ready and transfer failed
1 = device is ready and transfer succeeded
Bit 14 : STATE
0 = word received as DATA
1 = word received as HEADER
Bit 13 : PARITY, even parity in bits 15 to 0
Bit 12 : VALID
0 = transfer succeeded
1 = transfer failed
Bit 11-8 : Set to 0
Bit 7-0 : DATA

5.2 Interrupts

An interrupt line is provided to indicate a data change and avoid the need for the host to poll the eRED-MOD continuously. The interrupt line is an active low signal, asserted when one or more interrupt flags are set. There are 15 active high interrupt flag bits dispatched in the three registers. Refer to register definition for detailed information.

Interrupt flag bits are set when a change occurs in the related data. Interrupt flags must be cleared by the user software once the interrupt has been handled by the host. Writing a '0' clears the corresponding interrupt flag.

The interrupt line is deasserted when all interrupt flags are cleared.

5.3 Registers Types

Registers are entry points to access different types of data. There are two data types: BYTE and STRING.

BYTE is the simplest type and is used where a single data byte is needed, for instance with status register, volume control and volume level.

STRING type consists of a table of ASCII-encoded chars. As in standard C language, the last byte is a zero. When accessing a register that implements a string, BURST READ sequence must be used. STRING type is used for Artist/Album/Track Names and Track Format.

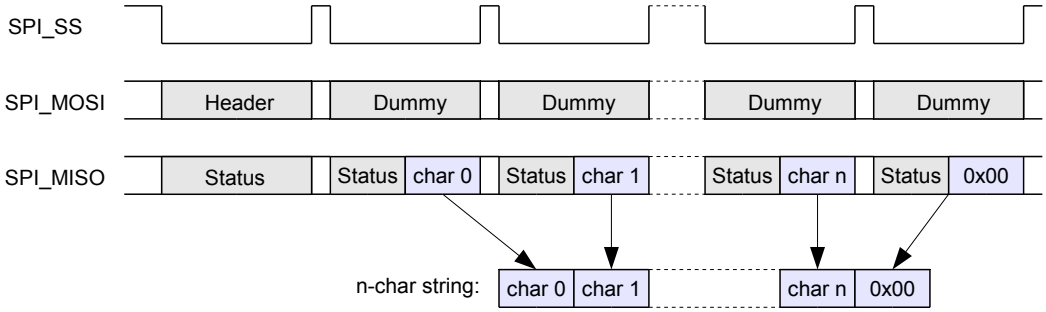

Figure 5-8 - STRING read sequence

5.4 Timing Requirements

SPI timing requirements are specified according to the following diagram.

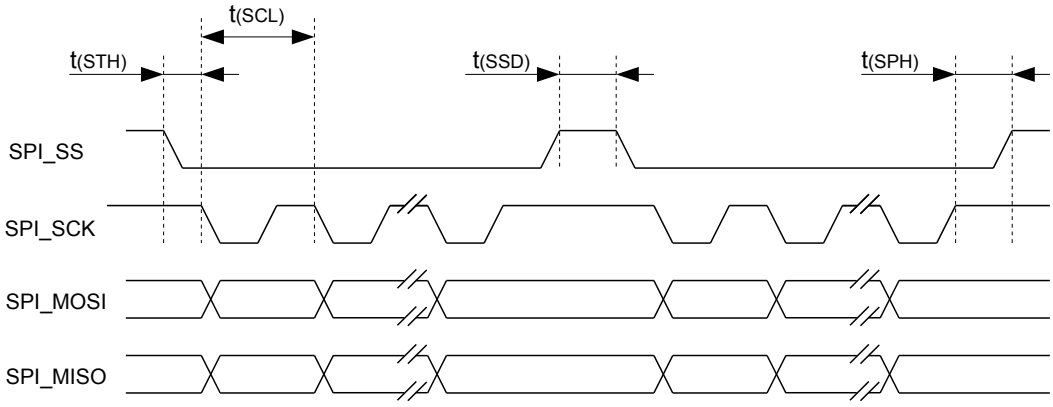

Figure 5-9 - SPI timing diagram

Parameter	Description	Min.	Max.	Unit
f_{SCLK}	Serial clock frequency		4	MHz
t_{SCLK}	Serial clock period duration	250		ns
t_{STH}	Hold time for start condition	50		ns
t_{SSD}	Slave Select de-assertion minimum time	7		µs
t_{SSD}	Slave Select de-assertion maximum time		500	ms
t_{SPH}	Hold time for stop condition		50	ns

Table 5-1 – SPI timing requirements

5.5 Register Map

Address	Name	Description	Direction	Type
0x40	VOL	Digital Volume Level	OUT	Byte
0x41	DVC	Digital Volume Control	IN	Byte
0x42	ETL	Elapsed Time LSB	OUT	Byte
0x43	ETH	Elapsed Time MSB	OUT	Byte
0x44	TDL	Track Duration LSB	OUT	Byte
0x45	TDH	Track Duration MSB	OUT	Byte
0x46	PS	Player Status	OUT	Byte
0x47	ARN	Artist Name	OUT	String
0x48	ALN	Album Name	OUT	String
0x49	TRN	Track Name	OUT	String
0x4B	TRF	Track Format	OUT	String
0x4C	IP0	IP Address byte 0	OUT	Byte
0x4D	IP1	IP Address byte 1	OUT	Byte
0x4E	IP2	IP Address byte 2	OUT	Byte
0x4F	IP3	IP Address byte 3	OUT	Byte
0x50	IF0	Interrupt Flags register 0	OUT	Byte
0x51	IF1	Interrupt Flags register 1	OUT	Byte
0x52	IF2	Interrupt Flags register 2	OUT	Byte
0x59	OFMT	Output Format	OUT	Byte
0x60	ELS	Ethernet Link Status	OUT	Byte
0x61	SR	Sample Rate	OUT	Byte
0x62	BPS	Bit Per Sample	OUT	Byte
0x65	SRT	SPI Read Test	OUT	Byte
0x66	SCR	Scratch	IN/OUT	Byte
0x68	MAC0	Ethernet MAC Address Byte 0	OUT	Byte
0x69	MAC1	Ethernet MAC Address Byte 1	OUT	Byte
0x6A	MAC2	Ethernet MAC Address Byte 2	OUT	Byte
0x6B	MAC3	Ethernet MAC Address Byte 3	OUT	Byte
0x6C	MAC4	Ethernet MAC Address Byte 4	OUT	Byte
0x6D	MAC5	Ethernet MAC Address Byte 5	OUT	Byte

Figure 5-10 - Register map

5.6 Registers Definition

This section provides details and bits definition for each register as well as their default setting after power-up.

5.6.1 Register 0x40 VOL

Description : Digital Volume Level
Type: : Byte, read-only
Details : Volume expressed in percent in a range of 0 to 100, 8-bit unsigned integer.
Default value : 100

5.6.2 Register 0x41 DVC

Description : Digital Volume Configuration
Type: : Byte
Details : Digital volume ON/OFF
Default value : 0x00 (Digital volume control enable)

DVC	7	6	5	4	3	2	1	0
Bit name	X	X	X	X	X	X	X	VDIS
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

VDIS : 1 = Digital volume control is disengaged
0 = Digital volume is active

5.6.3 Register 0x42 ETL

Description : Elapsed Time LSB
Type: : Byte, read-only
Details : Elapsed Time is expressed in seconds. This is a 16-bit unsigned integer value formed by the two bytes of registers ETH and ETL.

5.6.4 Register 0x43 ETH

Description : Elapsed Rime MSB
Type: : Byte, read-only
Details : Elapsed Time is expressed in seconds. This is a 16-bit unsigned integer value formed by the two bytes of registers ETH and ETL.

5.6.5 Register 0x44 TDL

Description : Track Duration LSB
Type: : Byte, read-only
Details : The Track Duration is expressed in seconds. This is a 16-bit unsigned integer value formed by the two bytes of registers TDH and TDL.

5.6.6 Register 0x45 TDH

Description : Track Duration MSB
Type: : Byte, read-only
Details : The Track Duration is expressed in seconds. This is a 16-bit unsigned integer value formed by the two bytes of registers TDH and TDL.

5.6.7 Register 0x46 PS

Description : Player Status
Type: : Byte, read-only

PS	7	6	5	4	3	2	1	0
Bit name	X	X	X	X	X	X	PS0	PS1
Access Type	R	R	R	R	R	R	R	R

PSx : 00 = stopped
01 = playing
10 = paused

5.6.8 Register 0x47 ARN

Description : Artist Name
Type: : String, read-only
Details : The Artist Name is a String composed of ASCII-encoded printable characters and terminated by a null character.

5.6.9 Register 0x48 ALN

Description : Album Name
Type: : String, read-only
Details : The Album Name is a String composed of ASCII-encoded printable characters and terminated by a null character.

5.6.10 Register 0x49 TRN

Description : Track Name
Type: : String, read-only
Details : The Track Name is a String composed of ASCII-encoded printable characters and terminated by a null character.

5.6.11 Register 0x4B TRF

Description : Track Format
Type: : String, read-only
Details : The Track Format is a String composed of ASCII-encoded printable characters and terminated by a null character.

5.6.12 Register 0x4C IP0

Description : IP Address byte 0
Type: : Byte, read-only
Details : The IP address is made of four registers according to the structure IP3.IP2.IP1.IP0

5.6.13 Register 0x4D IP1

Description : IP Address byte 1
Type: : Byte, read-only
Details : The IP address is made of four registers according to the structure IP3.IP2.IP1.IP0

5.6.14 Register 0x4E IP2

Description : IP Address byte 2
Type: : Byte, read-only
Details : The IP address is made of four registers according to the structure IP3.IP2.IP1.IP0

5.6.15 Register 0x4F IP3

Description : IP Address byte 3
Type: : Byte, read-only
Details : The IP address is made of four registers according to the structure IP3.IP2.IP1.IP0

5.6.16 Register 0x50 IF0

Description : Interrupt Flags Register 0
Type: : Byte

IF0	7	6	5	4	3	2	1	0
Bit name	X	TRN	ALN	ARN	PS	TD	ET	VOL
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

VOL : Volume changed
ET : Elapsed Time changed
TD : Track Duration changed
PS : Player Status changed
ARN : Artist Name changed
ALN : Album Name changed
TRN : Track Name changed

5.6.17 Register 0x51 IF1

Description : Interrupt Flags Register 1
Type: : Byte

IF1	7	6	5	4	3	2	1	0
Bit name	X	X	MAC	BPS	SR	ELS	IP	TFR
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TRF : Track Format changed
IP : IP address changed
ELS : Ethernet Link Status changed
SR : Sample Rate changed
BPS : Bits per sample changed
MAC : MAC address changed

5.6.18 Register 0x52 IF2

Description : Interrupt Flags Register 2
Type: : Byte

IF2	7	6	5	4	3	2	1	0
Bit name	X	X	X	X	X	X	X	OFT
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OFT : Output Format changed

5.6.19 Register 0x59 OFMT

Description : Output Format
Type: : Byte, read-only

OFMT	7	6	5	4	3	2	1	0
Bit name	X	X	X	X	X	X	X	DSD
Access Type	R	R	R	R	R	R	R	R

DSD : 1 = Output format is DSD
0 = Output format is PCM

5.6.20 Register 0x60 ELS

Description : Ethernet Link Status
Type: : Byte, read-only

ELS	7	6	5	4	3	2	1	0
Bit name	X	X	X	X	X	X	X	ELS
Access Type	R	R	R	R	R	R	R	R

ELS : 1 = Link is up
0 = Link is down

5.6.21 Register 0x61 SR

Description : Sampling Rate
Type: : Byte, read-only

SR	7	6	5	4	3	2	1	0
Bit name	X	X	X	X	X	SR2	SR1	SR0
Access Type	R	R	R	R	R	R	R	R

SR2x : 000 = 44.1kHz
001 = 48kHz
010 = 88.2kHz
011 = 96kHz
100 = 176.4kHz
101 = 192kHz
110 = 352.8kHz
111 = 384kHz

5.6.22 Register 0x62 BPS

Description : Bits per Sample
Type: : Byte, read-only

BPS	7	6	5	4	3	2	1	0
Bit name	X	X	X	X	X	X	BPS1	BPS0
Access Type	R	R	R	R	R	R	R	R

BPSx : 00 = 16-bit
01 = 24-bit
10 = 32-bit

5.6.23 Register 0x65 SRT

Description : SPI Read Test
Type: : Byte, read-only
Details : Register used for debugging purpose, fixed at 0xA5
Default value : 0xA5

5.6.24 Register 0x66 SCR

Description : Scratch
Type: : Byte
Details : Register used for debugging purpose, read and write access.
Default value : 0x00

5.6.25 Register 0x68 MAC0

Description : MAC Address byte 0
Type: : Byte, read-only
Details : The MAC address is made of six registers according to the structure MAC0:MAC1…MAC5

5.6.26 Register 0x69 MAC1

Description : MAC Address byte 1
Type: : Byte, read-only
Details : The MAC address is made of six registers according to the structure MAC0:MAC1…MAC5

5.6.27 Register 0x6A MAC2

Description : MAC Address byte 2
Type: : Byte, read-only
Details : The MAC address is made of six registers according to the structure MAC0:MAC1…MAC5

5.6.28 Register 0x6B MAC3

Description : MAC Address byte 3
Type: : Byte, read-only
Details : The MAC address is made of six registers according to the structure MAC0:MAC1…MAC5

5.6.29 Register 0x6C MAC4

Description : MAC Address byte 4
Type: : Byte, read-only
Details : The MAC address is made of six registers according to the structure MAC0:MAC1…MAC5

5.6.30 Register 0x6D MAC5

Description : MAC Address byte 5
Type: : Byte, read-only
Details : The MAC address is made of six registers according to the structure MAC0:MAC1…MAC5

6 Mechanical Data

6.1 Module mechanical specifications

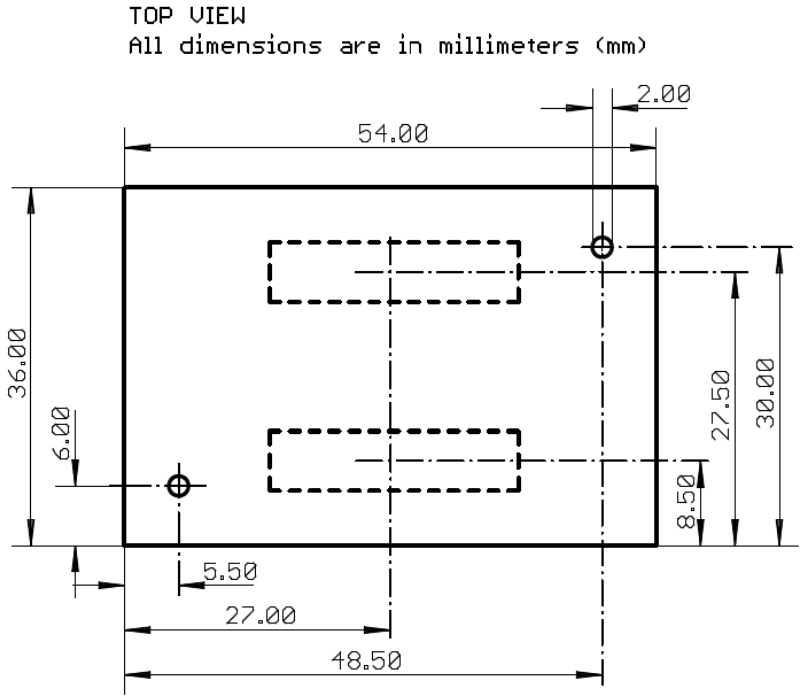

Figure 6-1 – Module dimensions

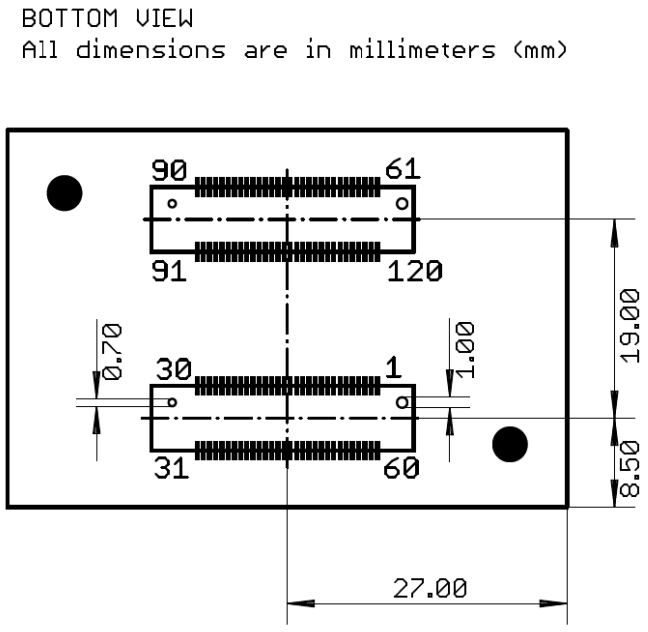

Figure 6-2 – Module bottom view

7 Ordering Information

7.1 Part Number

Part Number	Description
eRED-MOD	Network Audio Renderer

7.2 Kits and evaluation platforms

engineered offers various solutions to evaluate the eRED-MOD streaming technology in full-digital and analog audio environments.

The eRED-DOCK board is mainly a backplane for the eRED-MOD module with on-board clock management and facilitated connections. It provides digital audio signals and control flags on standard connectors, high quality master clock, isolated S/PDIF and AES/EBU output for easy evaluation.

Please check www.engineered.ch for latest information about evaluation boards availability.