Q8

UPSAMPLER

DATASHEET

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Preface

I. About This Datasheet

This document provides the information needed to design and integrate the Q8 Upsampler Module into your product. For more information, please refer to the product description available from the engineered Web site at: www.engineered.ch

II. Company Information

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Product specifications are subject to change without notice.

1 Introduction

1.1 Highlights

The Q8 Module is an ultra-high performance 2-channel Upsampler designed for high end, pro and consumer audio applications. Key features for the Q8 Module include:

- Superior performance asynchronous 24-bit/384kHz upsampling based on an enhanced version of the patented Q5 technology.
- Integrates with DSS™ synchronization technology for efficient jitter rejection.
- 384kHz upsampled digital output for driving 2 DAC's in dual mono mode.
- Additional direct down sampled 1x / 2x / 4x FS output port.
- DSD to PCM conversion.
- DoP decoding.
- Automatic input sampling frequency sensing.
- Supports sample rates input from 44.1kHz to 384kHz and word length from 16- to 24-bit.
- Input format: I2S or 2-channel DSD.
- Standalone hardware and configurable software modes available.
- Parameters available through SPI access.
- Compatible with Q5 Module.

1.2 Functional Block Diagram

The Q8 Module integrates four key technologies: Sonic Upsampling (enhanced version of the patented Q5), DSS™ Synchronization and DSF™ filtering to deliver a highly integrated asynchronous upsampler and digital synchronizer with best low-level signal. The module features a single audio input port capable of supporting PCM data up to 24-bit from frequencies up to 384kHz or stereo DSD64 (2.8224MHz) and DSD128 (5.6448MHz). In either case, the DSD signal or the direct PCM input are upsampled to a common 8x FS PCM format.

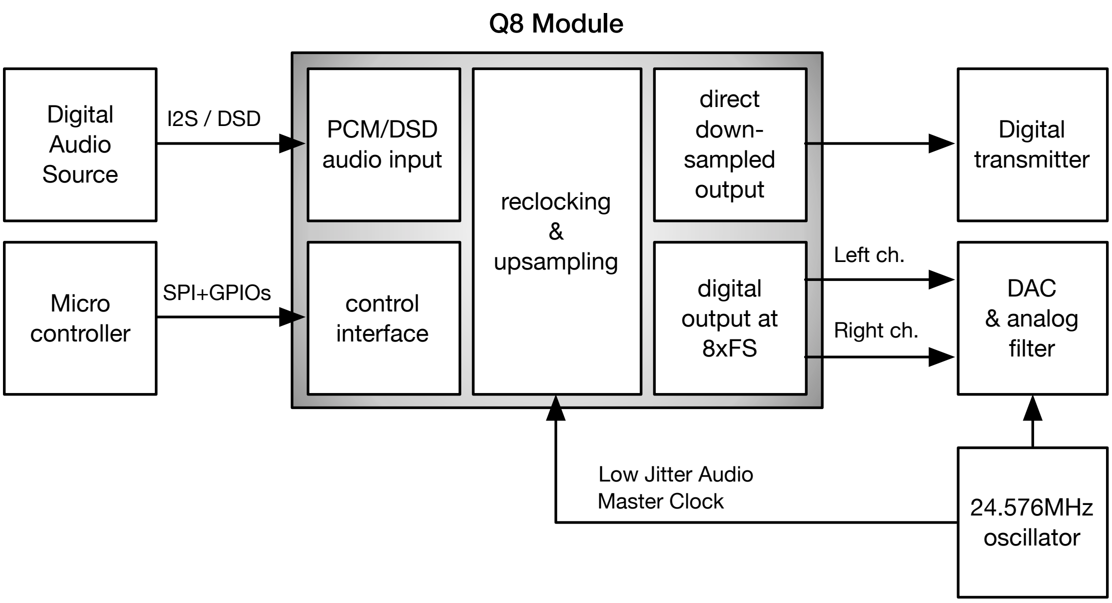

Figure 1-1 - functional block diagram

1.3 Sonic Upsampling

The Q8 Upsampler Module includes several proprietary technologies: adaptive time filtering, data-to-system synchronization, and an innovative virtual time-domain model. These technologies effectively reduce noise artefacts caused by imperfect digital systems and allow the digital signal to closer represent the true analog sound of the studio mastered audio data.

Adaptive time filtering allows the system to adapt to small fluctuations in the systems audio master clock. The master clock is the heart of any digital audio system, however as all components that are constructed from physical materials, they will at some point in time deviate from their ideal generalized behaviour causing, in this case variation in frequency and system jitter in this important internal timing reference. Typically, these variations will not be corrected for, however in Q8 enabled devices the system automatically adapts to these small fluctuations resulting in perfect “glitch” free analog sound even after endless hours of continuous playback.

Data-to-System synchronization allows any incoming audio stream to be resynchronized and retimed to a local high quality clock. By using a stable clock reference, the negative effects of inter-component jitter can be minimized. When converting the digital audio to an analog signal through high performance D/A converters, this reduction in jitter has enormous benefits in the level of detail and clarity in the reconstructed analog sound. Combing this process with a virtual time domain model that uses an advanced cubic interpolation algorithm to resample the incoming audio data, timing errors in this signal can be compensated for at amazing levels of accuracy. The result is a tighter and more focused bass, an increased stereo imaging, as well as clarity and separation for all musical instruments and voices.

1.4 DSD to PCM Conversion

The Q8 Module can use a Direct Stream Digital (DSD) audio stream at 2.8224MHz or 3.072MHz (64x 44.1kHz or 48kHz), 5.6448MHz or 6.144MHz (128x 44.1kHz or 48kHz) as input audio source. A DSD stream is a one-bit delta-sigma modulated digital audio signal sampled in a sequence of very high frequency. This format is used to store audio on Super Audio Compact Disc (SACD) and is now popular on high-resolution music available for download. Audio processing of the input DSD stream inside the Q8 Module is done by first converting the DSD data to PCM format thanks to the DSF™ Filtering, then using standard PCM audio processing techniques. The audio channel configuration supported by the Q5 Module is 2-channel stereo DSD.

For seamless audio format integration, DoP (DSD over PCM) encoded input streams are automatically detected and decoded. Detection is based on the specific DoP marker code. Stereo DSD data are then extracted from the pseudo PCM data stream and sent to the DSD to PCM converter unit.

1.5 DSF™ Filtering

Due to its very high sampling rate (2.8224MHz, 3.072MHz, 5.6448MHz or 6.144MHz) and one-bit nature, DSD is incompatible with already implemented signal processing functions targeting standard PCM data. The Direct Stream Filtering (DSF™ Filtering) algorithm converts DSD streams to PCM up to 8x FS with superb quality. The Q8 Module integrates this feature in order to supply very high audio quality from a DSD 64 or DSD 128 audio stream and therefore significantly enhances performance of any audio applications using this single-bit encoding.

2 Characteristics and Specifications

2.1 Electrostatic Discharge Warning

Many of the components in this product are subject to be damaged by electrostatic discharge (ESD). Customers are advised to observe proper ESD precautions when unpacking and handling the board, including the use of a grounded wrist strap at an approved ESD workstation.

Caution: Failure to observe ESD handling procedures may result in damage to the device.

2.2 Recommended Operating Conditions

Table 2-1 indicates the recommended conditions under which the product should run properly.

Parameter	Recommend Condition	
Power supply voltage	3.30V DC	
Input signal voltage	$V_{IL\ (min/max)}$: 0.0V / 0.5V	$V_{IH\ (min/max)}$: 2.4V / 3.3V
Operating free-air temperature	$T_{A(min/max)}$: 0°C / 60°C	

Table 2-1 - recommended operating conditions

2.3 Absolute Maximum Ratings

The user should be aware of the absolute maximum operating conditions for the Q8 Module. Stress beyond maximum ratings may cause permanent damage to the device. Table 2-2 summarizes the critical data points.

Parameter	Min.	Max.
Power supply voltage	-0.30V	3.60V
Input signal voltage	-0.30V	3.60V
Input current (any pins excepts supplies)	-10mA	+10mA
Output signal load impedance	180Ω	-
Operating free-air temperature	-20°C	60°C
Storage temperature	-20°C	85°C

Table 2-2 - absolute maximum ratings

2.4 Electrical Specifications

Parameter	Min.	Typ.	Max.
DC supply voltage	3.10V	3.30V	3.60V
DC supply current		350mA	500mA
Input logic level high V_{IH}	2.4V		
Input logic level low V_{IL}			0.5V
Input logic current	-0.5mA		0.5mA
Output logic level high V_{IH}	V_{DD} - 0.6V	3.10V	V_{DD}
Output logic level low V_{IL}	0	0.2V	0.4V
Output logic current	-15mA		15mA

Table 2-3 - electrical specifications

2.5 Digital Audio Specifications

Parameter	Min.	Typ.	Max.
Master clock input frequency		24.5760MHz	
PCM input resolution	16-bit		24-bit
PCM input sample rate	44.1kHz		384kHz
PCM input format		I2S	
DSD input frequency	2.8224MHz		6.144MHz
DSD input format		2-channel 1-bit DSD (direct stream digital)	
TX0 PCM output format		I2S	
TX0 PCM output clocking		master	
TX0 PCM output sample rate		1x FS (48kHz) / 2x FS (96kHz) / 4x FS (192kHz)	
TX1 PCM output format		mono-framed left-justified mode / mono-framed right-justified mode	
TX1 PCM output clocking		master	
TX1 PCM output sample rate		384kHz	
Dynamic range		24-bit	
THD+N	-140dB	-144dB	-147dB

Table 2-4 – digital audio specifications

2.6 Pin assignments

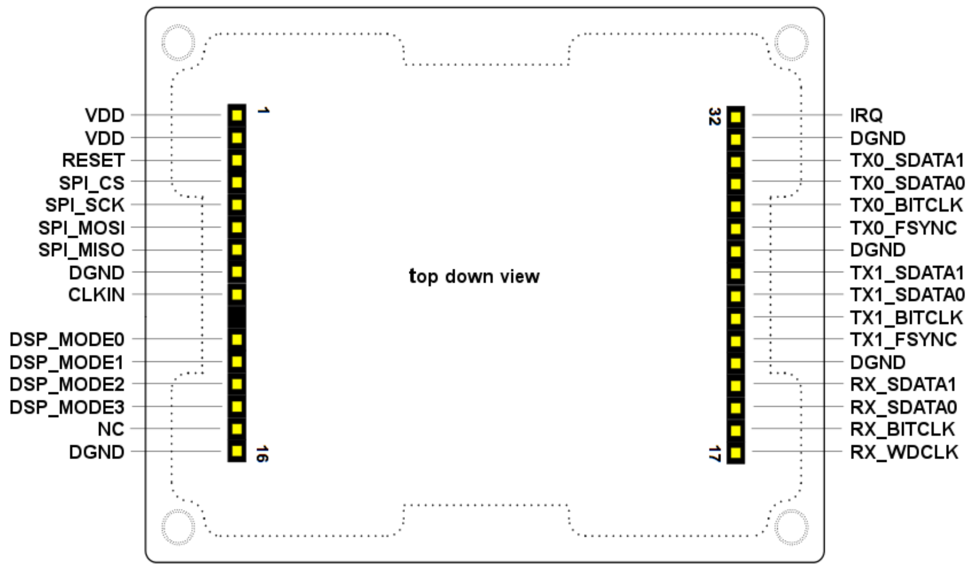

Figure 2-1 - pin assignments

2.7 Housing Dimensions

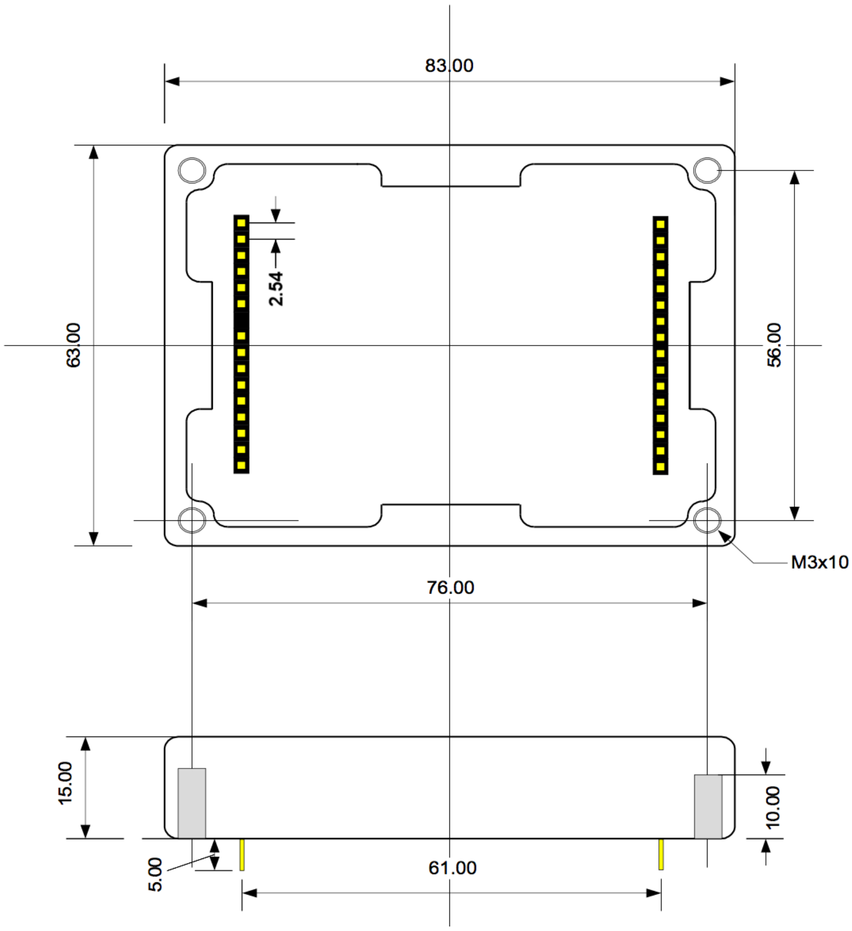

Figure 2-2 - housing dimensions

2.8 Pin descriptions

Pin #	Name	Type	Description
1	VDD	Power	Digital core and I/O power supply: +3.30V
2	VDD	Power	Digital core and I/O power supply: +3.30V
3	$\overline{\text{RESET}}$	Input	Reset – active low, internal pull-up resistor
4	$\overline{\text{SPI\_CS}}$	Input	Reset – active low, internal pull-up resistor
5	SPI_SCK	Input	Control port SPI clock
6	SPI_MOSI	Input	Control port SPI data input
7	SPI_MISO	Output	Control port SPI data output, open-collector, internal pull-up resistor
8	DGND	Ground	Digital core and I/O ground
9	CLKIN	Input	Master clock input
10	NC	Do not connect	Cut pin
11	DSP_MODE0	Input	TX1 output port data format Low: mono-framed left justified output mode High: mono-framed right justified output mode
12	DSP_MODE1	Input	DSD/PCM input format Low: PCM or DoP input stream High: native DSD input stream
13	DSP_MODE2	Input	Unused – connect to GND
14	DSP_MODE3	Input	Data Valid flag – active low Low: incoming audio data stream is valid High: incoming audio data stream is not valid, output is muted
15	NC	Do not connect	Reserved for factory use
16	DGND	Ground	Digital core and I/O ground
17	RX_WDCLK	Input	PCM serial audio input Word Clock Do not connect in DSD mode
18	RX_BITCLK	Input	PCM/DSD serial audio input Bit Clock
19	RX_SDATA0	Input	PCM serial audio input stereo data DSD serial audio input left channel data
20	RX_SDATA1	Input	DSD serial audio input right channel data
21	DNGD	Ground	Digital core and I/O ground
22	TX1_FSYNC	Input/Output	Serial audio output Frame Sync for TX1_SDATA0 and TX1_SDATA1
23	TX1_BITCLK	Input/Output	Serial audio output Bit Clock for TX1_SDATA0 and TX1_SDATA1
24	TX1_SDATA0	Output	Serial audio output Left Upsampled left mono channel PCM audio data serial output
25	TX1_SDATA1	Output	Serial audio output Right Upsampled right mono channel PCM audio data serial output
26	DNGD	Ground	Digital core and I/O ground
27	TX0_FSYNC	Input/Output	Serial audio output frame Sync for TX0_SDATA0 and TX0_SDATA1
28	TX0_BITCLK	Input/Output	Serial audio output Bit Clock for TX0_SDATA0 and TX0_SDATA1
29	TX0_SDATA0	Output	Serial audio output data Stereo Direct down-sampled stereo channel PCM audio data serial output pin
30	TX0_SDATA1	Output	Serial audio output data - reserved
31	DGND	Ground	Digital core and I/O ground
32	$\overline{\text{IRQ}}$	Output	Control port interrupt request – active low

Table 2-5 – pin descriptions

3 Interfacing and Operation

3.1 General Description

The Q8 Module is a 2-channel, asynchronous digital data stream upsampler with D/A conversion error minimization and multi-DAC data distribution. Operation at PCM input sampling frequencies from 44.1kHz to 384kHz, DSD at 2.8224MHz or 5.6448MHz and output at 384kHz are supported. Best-in-class dynamic range and THD+N are achieved by employing an innovative upsampling kernel with better than 147dB of image rejection. A direct down-sampling option allows for dual digital output ports driven at different sampling frequencies.

The audio input port supports the I2S standard and the 2-channel DSD audio data format while the output port is configured on mono-framed audio data format. Input word lengths from 16- to 24-bit are supported. Input ports are operated in Slave mode, deriving their word and bit clocks from external input devices. Output ports are operated in Master mode allowing the incoming data stream to be re-clocked and synchronized around a single high quality master clock, referred to as DSS synchronization. In the Master mode of the output ports, the FSYNC and BITCLK clocks are derived from the system master clock CLKIN.

The Q8 Module includes a four-wire SPI port, which is used to access on-chip control and status registers in Software mode. The SPI port facilitates interfacing to microprocessors or digital signal processors that support synchronous serial peripherals. In Hardware mode, dedicated control flags are provided for basic functions. These pins can be hard-wired or driven by logic or host control. In addition to the normal control interfaces, the Q8 Module provides an artefact-free soft mute function in software mode as well as automatic input frequency sensing.

3.2 Typical Connections

The Q8 Module can be operated in hardware mode whereby the SPI port (*) is not needed to configure the module but rather the FLAG pins. Please note that some features are accessed only by the SPI port therefore hardware mode offers reduced functionalities. Figure 3-1 illustrates typical connexions with digital audio receiver, a host MC, DAC's and digital transmitter.

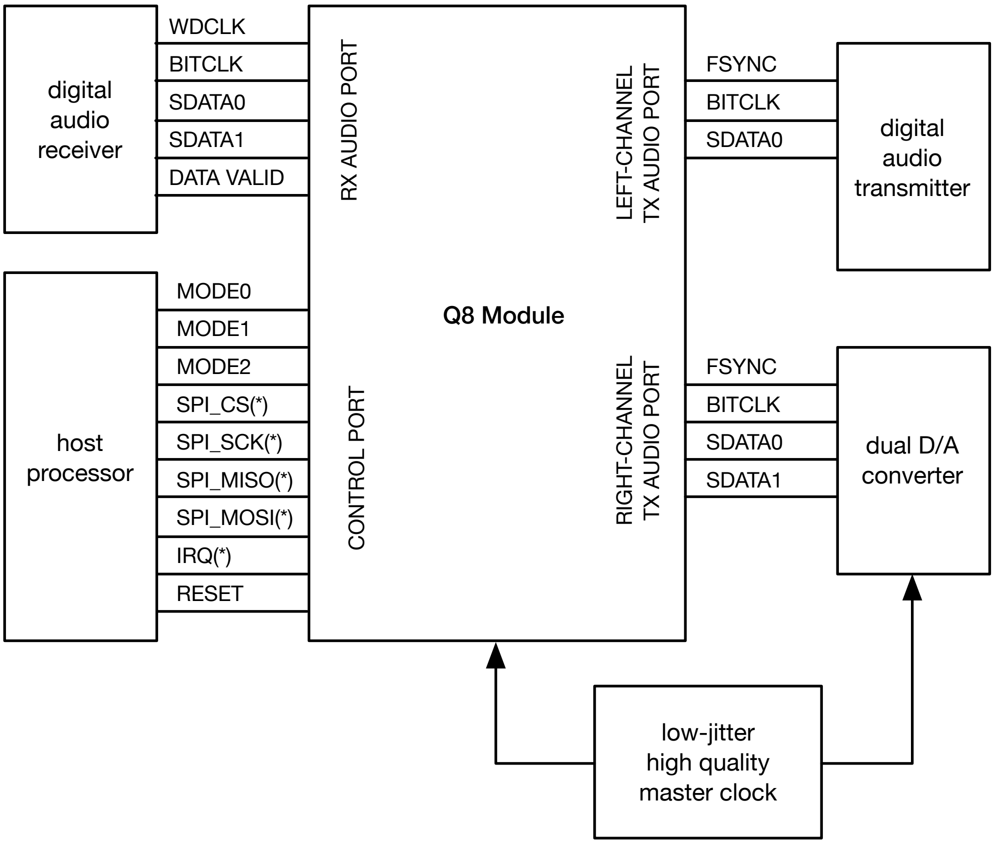

Figure 3-1 - typical connexions

3.3 Interfacing to Digital Audio Receivers

Audio input and output ports are designed to interface to a variety of audio devices, including receivers commonly used for AES/EBU and S/PDIF communications. Figure 3-2 illustrates the interface between a Cirrus Logic WM8804 receiver and the Q8 input port whereby the Q8 Module works as Slave and the receiver as Master.

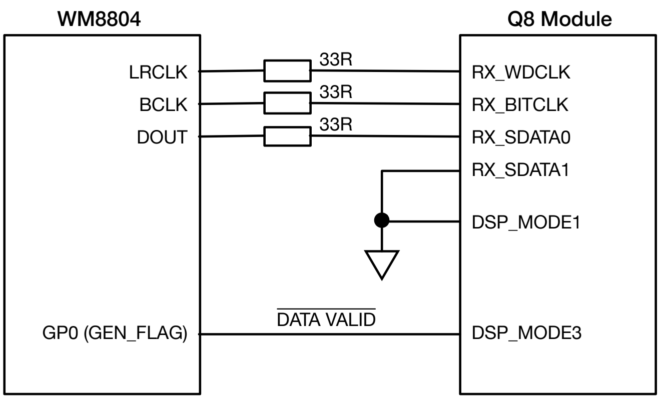

Figure 3-2 - interfacing with a digital receiver

Careful impedance matching must be maintained between drivers, transmission lines and receivers to minimize signal overshoot, undershoot or ringing. Figure 3-2 shows source damping-resistor terminations of 33R as an example. Proper impedance matching and termination depends upon design and layout.

In situation described in Figure 3-2 , DSP_MODE1 is low for PCM and DoP input support. A DoP encoded stream will be seen by the digital audio receiver as a PCM data flow, but the Q8 Module will detect it and extract DSD data. DSP_MODE3 is used for muting the Q8 output when the receiver is unlocked or transmitting non-audio data.

3.4 Interfacing Q8 outputs

The Q8 Module is designed specifically to drive high performance 384kHz D/A converters. Thus, the module is able to drive both dual 384kHz compatible DAC's and an external transmitter at the same time. Connection to dual DAC's, configured in mono mode, and to the transmitter is given in Figure 3-3. In that case the Q5 works as Clock Master and the DAC's / Transmitter as Clock Slave devices.

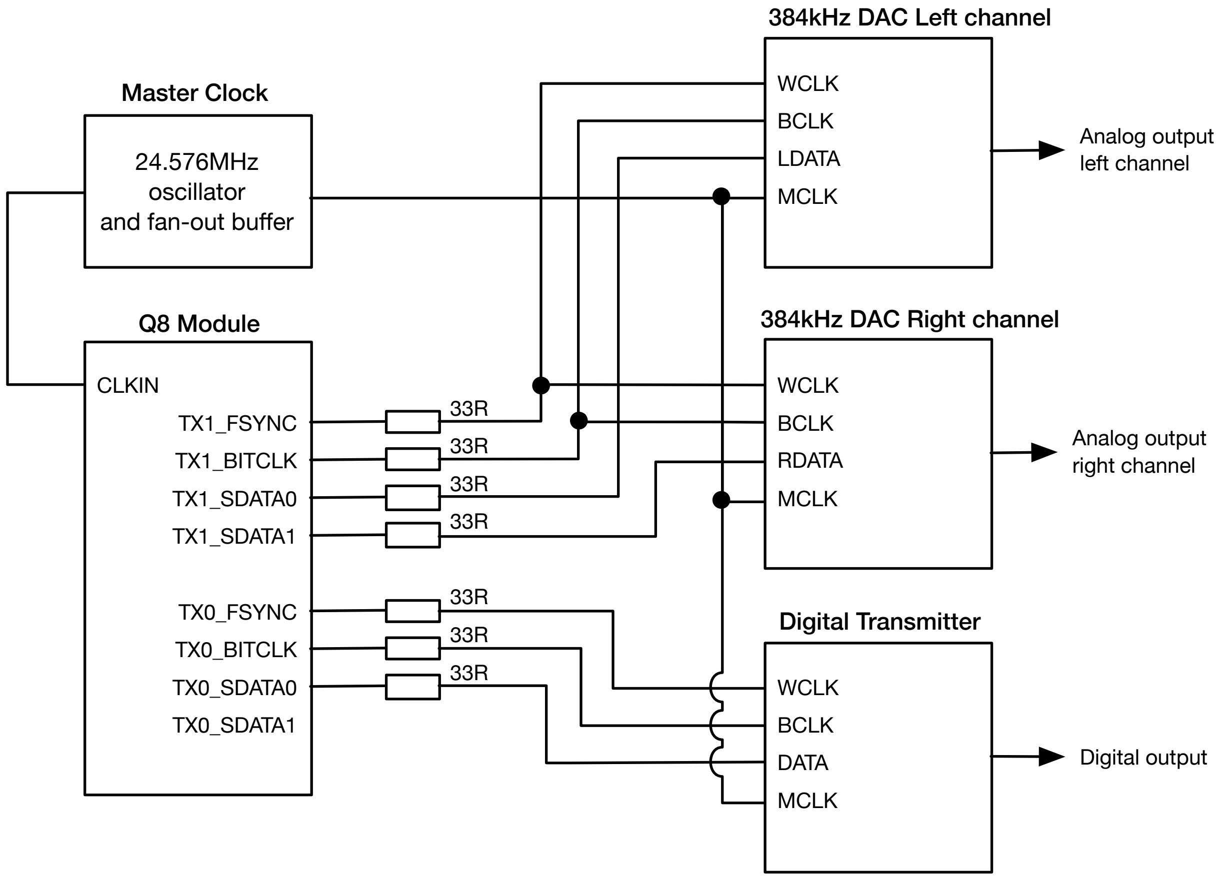

Figure 3-3 - interfacing to D/A converters

3.5 Reference Master Clock

The Q8 Module requires a low-jitter master clock for operation. This clock must be supplied at the CLKIN input (pin 9) directly from an external crystal oscillator or by a clock buffer. The Q8 Module is designed to work with a single frequency at 24.5760MHz. As a result, all the audio output sampling frequencies will be derived from a multiple of 48kHz.

Master clock distribution must be carefully designed to minimise jitter. Best result is usually achieved by using a clock fan-out buffer and point-to-point connexions to each device with proper impedance matching.

3.6 Reset and Power On

The Q8 Module may be reset using the $\overline{\text{RESET}}$ input (pin 3). It has to be held low for a minimum of 500ns to guaranty a proper reset. The $\overline{\text{RESET}}$ has an internal pull-up resistor. Furthermore, the Q8 integrates an internal power-on reset management, so the user doesn't need to force a reset sequence after power up in order to initialize the module.

Once the reset is released, there is a 400ms delay for the module to be operational. In software mode, the host MCU must observe this delay before attempting to write to the SPI port due to internal logic requirements.

3.7 Audio Serial Input Port (RX)

The RX audio input port is a four-wire synchronous serial interface working in Slave mode. In PCM mode, the port uses three signals, namely RX_WDCLK (pin 17), RX_BITCLK (pin 18) and RX_SDATA0 (pin 19). RX_WDCLK provides the frame synchronization clock while RX_DATA0 and RX_BITCLK are used to respectively transfer the serial audio data and clock the serial data into the port. This latter supports sampling frequencies up to 384kHz. The audio data word length may be up to 24bit and the audio data is always binary two's complement with the MSB first.

In DSD mode, three signals out of four are used, RX_BITCLK (pin 18), RX_SDATA0 (pin 19) and RX_SDATA1 (pin 20) pins. RX_BITCLK provides the DSD clock synchronization (2.8224MHz, 3.072MHz, 5.6448MHz or 6.144MHz) while RX_SDATA0 and RX_SDATA1 are respectively the left and right channel data. Figure 3-4 illustrates the audio data stream of each mode.

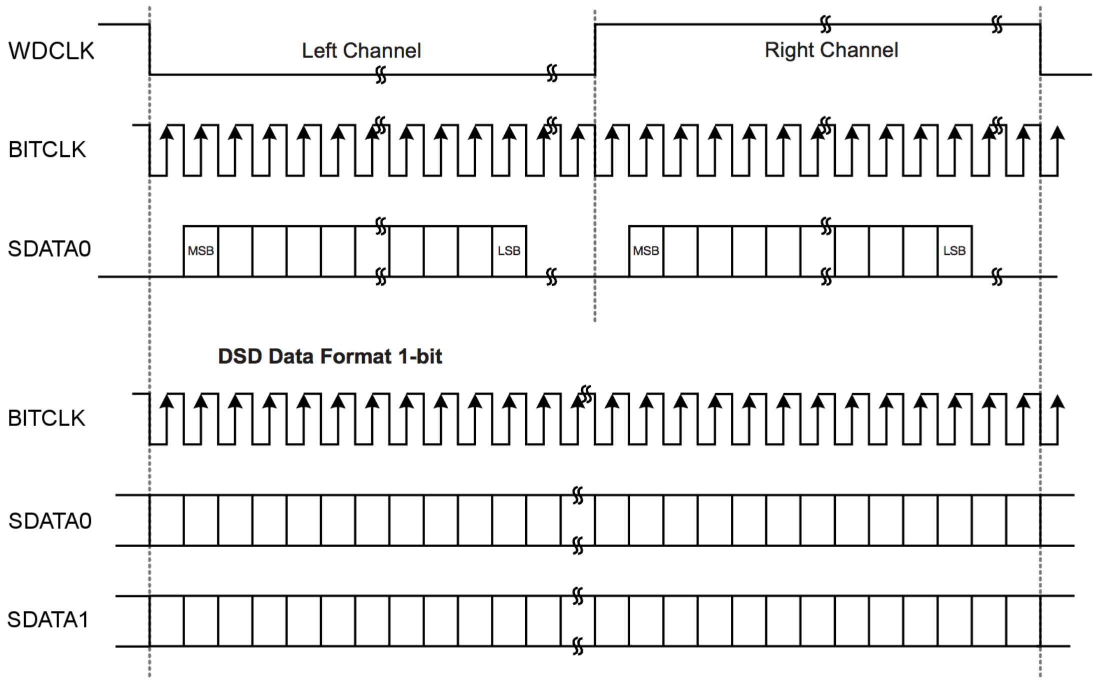

Figure 3-4 - audio input port data format

In software mode, the Input Control Register allows to select the input audio data format mode. Two bits are used to choose the mode, namely FMT0 and FMT1. The configuration in the Input Control register is OR-ed with the DSD Input pin DSP_MODE1.

In hardware mode, it is the DSD Input pin DSP_MODE1 that allows the input audio data format mode to be configured. When DSD Input pin is high, the DSD mode is selected as opposed to low where the PCM mode is enabled. DoP data and clocking is equivalent to PCM, therefore DSP_MODE1 must be low for DoP stream.

3.8 TX1 Audio Output Port

The TX1 audio output port is a four-wire synchronous serial interface working in Master mode. TX1_SDATA0 (pin 24) and TX1_SDATA1 (pin 25) pins are the PCM upsampled serial data output for left and right channels. TX1_BITCLK (pin 23) output operates at a rate of 32x FSYNC. The Word Clock TX1_FSYNC (pin 22) is also configured as output and is set to operate at a rate of 8x FS.

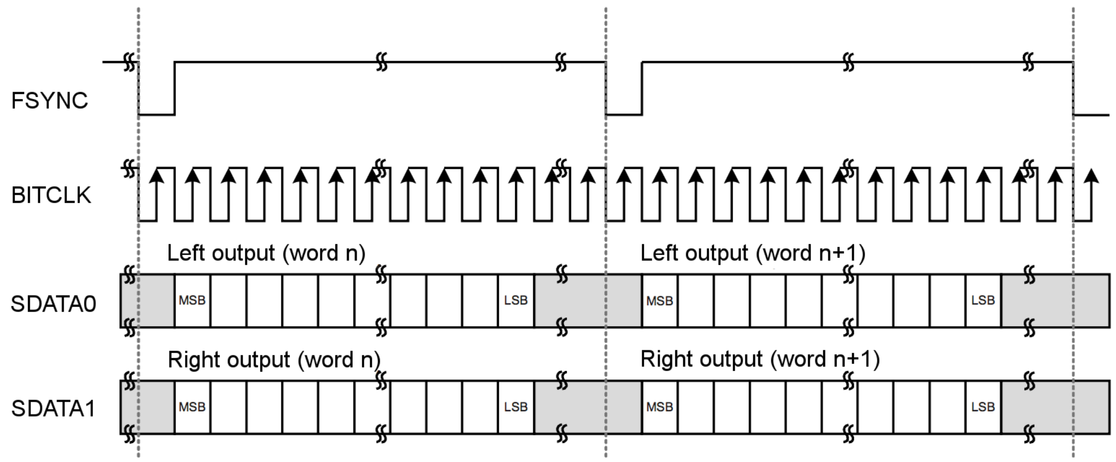

Figure 3-5 - MonoFramed DSP Mode

The audio output ports are configured either in MonoFramed DSP Mode or MonoFramed Right-Justified Mode. The audio data word length is set to 32-bit. The audio data is always Binary Two's Complement with the MSB first. Refer to Figure 3-5 and Figure 3-6 for the output data formats.

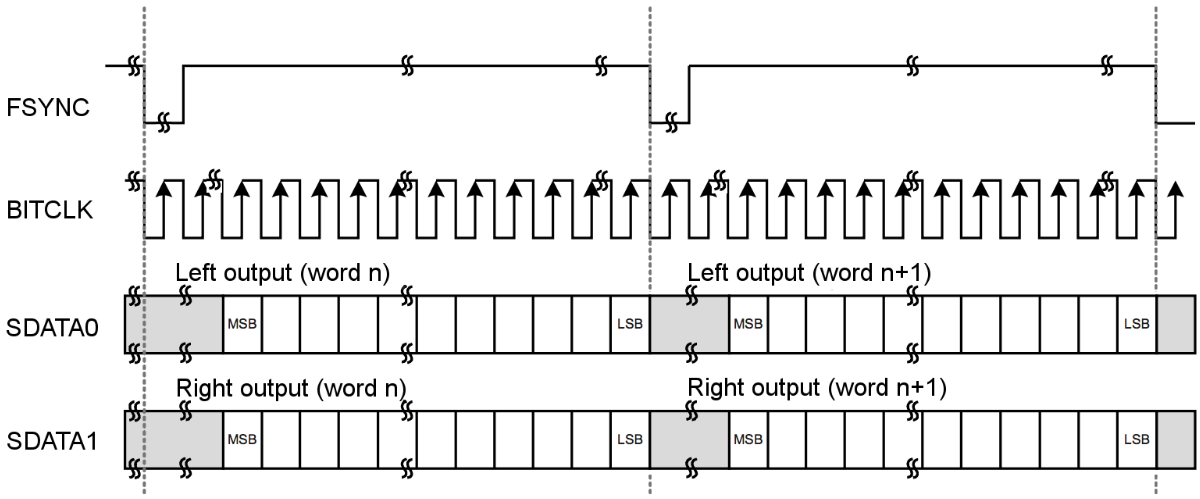

Figure 3-6 - MonoFramed Right-Justified DSP Mode

3.9 TX0 Audio Output Port

TX0 audio output port is a three-wire synchronous serial interface working in I2S Master mode. TX0_SDATA0 (pin 29) output is the PCM down-sampled serial data output. The left/right word clock referred to as frame sync, TX0_FSYNC (pin 27) output pin can be set to operate at rates of 1x FS, 2x FS or 4x FS.

The audio data word length is 32-bit. The audio data is always Binary Two's Complement with the MSB first. Refer to Figure 3-7.

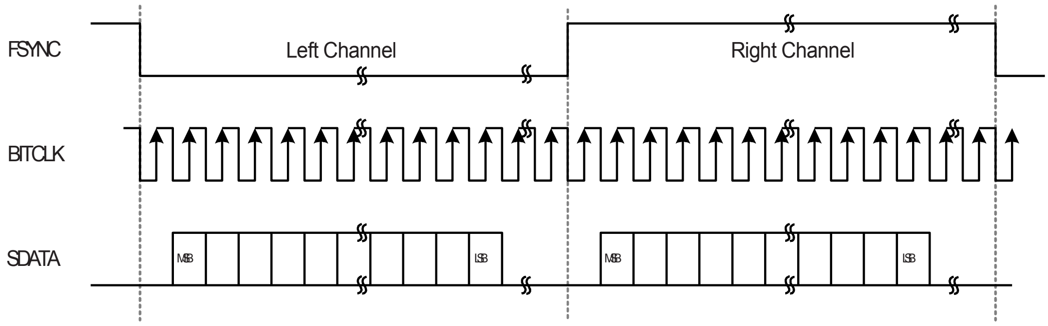

Figure 3-7 - TX0 Output data format

3.10 Data Resolution and Dither

When using the serial audio input port in I2S mode, all input data is processed as 32-bit wide. Any audio data width truncation (compared to the original audio data source), performed prior to the Q8 Module, should have been done using an appropriate dithering process. There is no dithering mechanism on the input side of the Q8 Module, so care must be taken to ensure that no truncation occurs. The audio output ports are set to 32-bit.

3.11 Incoming Sampling Rate and Locking

When the Q8 Module processes the incoming audio data stream, it calculates the ratio between the input and output sample rates and uses this information to set up various internal parameters. In PCM input mode, the Q8 Module accepts standard sampling frequencies of 32, 44.1, 48, 88.4, 96, 176.4, 192, 352.8 and 384kHz with a ±2% deviation from the nominal value. Whereas in DSD input mode, the Q8 Module accepts sampling frequencies of 2.8224, 3.072, 5.6448 and 6.144MHz with a ±2% deviation from the nominal value. If a non-standard input sampling frequency is found or the standard sampling rate deviates more than 2% from the nominal value, the Q8 Module will NOT process the incoming data and will be a status of unlocked.

The Q8 Module can dynamically compensate for drift and fluctuations in the incoming input sampling frequency where the processing will track the incoming sample rate and automatically adjust the sample rate conversion process in order to maintain the highest level of audio quality.

In Software mode, Input Control Register functions as status registers, which contains the input frequency sampling detected. The INTREQ pin reflects the lock state of the module. If there is a change in the input sampling rate the INTREQ signal goes low to indicate an unlock state until the Q8 Module reacquires a valid ratio. At this point, the INTREQ will transition high.

3.12 Muting

The TXx_SDATA0, TXx_SDATA1, TXx_BITCLK and TXx_FSYNC pins are all low (hard mute) when module is either in reset state or unlocked (no audio source or Data Valid flag high). These pins become valid as soon as the Q8 Module gets locked.

When the module is locked, TXx_SDATA0, TXx_SDATA1 pins can be set to all zero by applying a soft mute through the configuration of the "Mute" bit in the SPI process control register. In this case TXx_BITCLK and TXx_FSYNC are still active. Thus, in hardware mode, only the Data Valid flag pin can be used whereas in software mode, there are two ways to put the module in mute, which are the Data Valid flag or the "Mute" bit in the SPI register.

3.13 Phase Inversion

The Q8 Module includes a phase inversion function whereby the output data can be inverted compared with audio input signal. By default, this function is disabled and can only be enable in software mode. The selected configuration can be changed through the LSB bit called PHI of the Process Control Register. All other features of the module don't affect this function.

3.14 Stereo DSD to PCM Conversion

The Q8 Module includes a stereo DSD to PCM converter. This gives the possibility of connecting a DSD input stream on the RX input port and using this stream as main audio source. The selection of the DSD input format is done by setting DSP_MODE1 pin in hardware. In software mode, the FMT bits in Input control register allows to enable the DSD input format.

As described in chapter 3.7 "Audio Serial Input Port (RX)", the RX audio input port is a four-wire synchronous serial interface that is configured to operate in Slave Mode. Only three out of four lines are used. The RX_SDATA0 and RX_SDATA1 lines are the serial audio data inputs for DSD left and right channels respectively. DSD data format is 1bit stream, therefore no frame synch is needed.

DoP (DSD over PCM) is received by the input port RX as a PCM stream and accordingly DSP_MODE1 must be low. DoP encoded input stream is automatically detected by the PCM input unit according to the specific DoP marker code. Stereo DSD data are then extracted from the pseudo PCM data stream and sent to the DSD to PCM converter unit.

3.15 Data Valid flag (DSP_MODE3)

The Q8 Module uses the Data Valid flag (DSP_MODE3) input pin to know whether it should attempt to synchronize with the incoming audio data stream. If the Data Valid flag is high, then the module will never attempt to lock and the outputs will be hard muted. If the Data Valid flag is low, then the module will attempt to find the input sampling frequency and process the audio data as long as they are valid. The INTREQ pin can be used to track the module state (lock / unlock).

3.16 Serial Port Interface (SPI Port)

The SPI port is the interface used to operate the Q8 Module in software mode. This port allows the system host MCU to access Q8 Module internal registers for read and write operations. The host MCU is referred as the Master Device and the Q8 Module is referred as Slave Device.

The operation of the SPI port may be completely asynchronous with respect to the audio stream rates. However, it is recommended to keep the port pins static if no operation is required.

The SPI port is a four-wires serial interface where $\overline{\text{SPI\_CS}}$ (active low) is the module chip select signal, SPI_SCK is the control port bit clock (input into the module from the Master Device), SPI_MOSI is the input data line from Master Device and SPI_MISO is the output data line to the Master Device. Data is clocked in on the rising edge of SPI_SCK and clocked out on the falling edge.

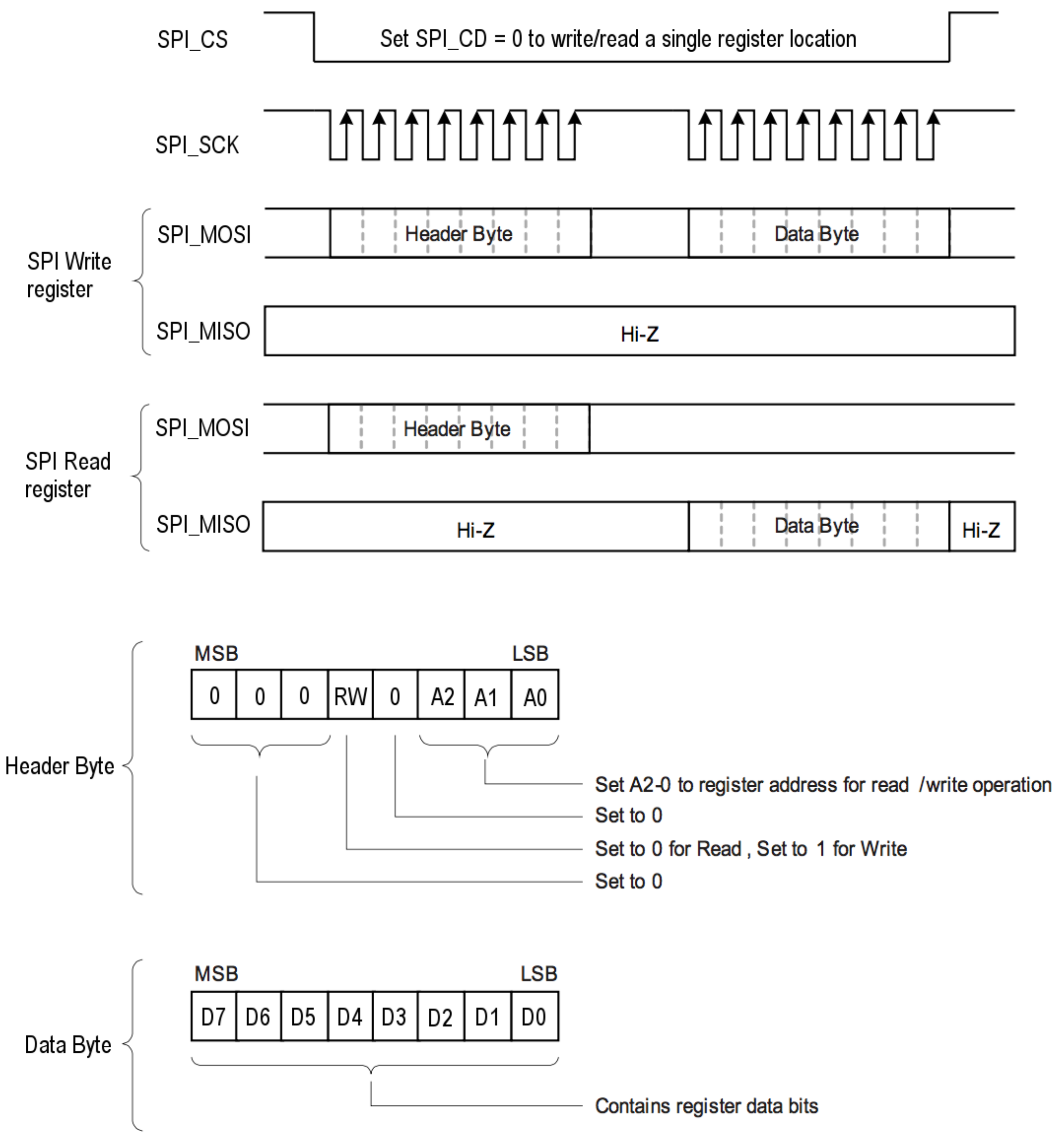

Figure 3-8 - SPI protocol for register read/write operations

Table 3-1and Figure 3-8 illustrate the operation of the SPI port as well as the protocol for register read and write operations.

Byte Name	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Header Byte	0	0	0	RW	0	A2	A1	A0
Data Byte	D7	D6	D6	D4	D3	D2	D1	D0

Table 3-1 - SPI byte definition for register read/write operations

A2 – A0 Register address selection

RW Read/Write control
0: Register Read
1: Register Write

D0 – D7 Register data

4 Hardware Mode

4.1 General Description

The Q8 Module can work in hardware mode which allows the device to operate without a host system or serial communication on the SPI port. The device is considered in Hardware mode when the MD_CS pin is left unconnected or pulled up with a resistor (10kΩ) to VDD. In this mode, the module starts in a default configuration. However, the four DSP_MODEx pins remain valid and are used for setting the Q8 Module in the correct operation mode.

4.2 Hardware Configuration

To work in hardware mode, the SPI port can be left unconnected. DSP_MODEx pins are described here below.

Pin #	Name	Type	Description
11	DSP_MODE0	Input	TX1 Output port data format
12	DSP_MODE1	Input	DSD/PCM input format
13	DSP_MODE2	Input	Unused – should be connected to GND
14	DSP_MODE3	Input	Data Valid flag – active low

Table 4-1 - DSP-MODEx hardware control summary

DSP_MODE0 TX1 output port data format
0: mono-framed left justified output mode
1: mono-framed right justified output mode

DSP_MODE1 DSD/PCM input format
0: PCM or DoP input stream
1: native DSD input stream

DSP_MODE2 Unused – should be tied to GND

DSP_MODE3 Data Valid flag
0: incoming audio data stream is valid
1: incoming audio data stream is not valid, output is muted

5 Software Mode

5.1 General Description

The Q8 Module software mode requests the device to operate with a host system having an SPI port. This mode allows the host system to configure or read information from the Q8 Module by accessing its internal registers through the SPI port (see chapter 3.16 “Serial Port Interface (SPI Port)” for further details on SPI operational port). The following chapters give details and bits definition of each register as well as their default setting after reset.

Q8 Module Registers Overview

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	Input Status	SFMT0	x	XFS3	XFS2	XFS1	XFS0	FMT1	FMT0
0x01	TX0 Output Control	x	x	x	x	TX01	TX00	x	x
0x02	Process Control	x	x	x	x	x	DATA	MUTE	PHI
0x03	*Reserved for factory use*	-	-	-	-	-	-	-	-
0x04	*Reserved for factory use*	-	-	-	-	-	-	-	-
0x05	*Reserved for factory use*	-	-	-	-	-	-	-	-
0x06	Software Revision	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
0x07	Product ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0x08	*Reserved for factory use*	-	-	-	-	-	-	-	-
0x09	Sub Product ID	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0

Table 5-1 – register map

5.2 Input Status Register

Register address: 0x00

	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Bit name	SFMT0	x	XFS3	XFS2	XFS1	XFS0	FMT1	FMT0
Access type	R	R	R	R	R	R	R	R
Default value	0	0	0	0	0	0	0	0

FMT 1..0 Input Format
00: I2S
01: reserved
10: reserved
11: DSD

XFS 3..0 Input Sampling Frequency
0000: Unlock
0001: 32kHz
0010: 44.1kHz
0011: 48kHz
0100: 88.2kHz
0101: 96kHz
0110: 176.4kHz

0111: 192kHz
1000: 352.8kHz
1001: 384kHz

SFMT0 Input Sub Format
0: PCM
1: DoP (PCM frame containing encapsulated DSD data)

5.3 TX0 Output Control Register

Register address: 0x01

	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Bit name	x	x	x	x	TX01	TX00	x	x
Access type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	0	0	0	0	0	1	0	0

TX01..0 Direct down-sampled output frequency
00: *Reserved*
01: 1x FS (48kHz)
10: 2x FS (96kHz)
11: 4x FS (192kHz)

5.4 Process Control Register

Register address: 0x02

	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Bit name	x	x	x	x	x	DATA	MUTE	PHI
Access type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	0	0	0	0	0	0	0	0

PHI Phase Inversion
0: Phase inversion OFF
1: Phase inversion ON

MUTE Audio output ports mute
0: Mute OFF
1: Mute ON

DATA Data Input Mode
0: 352.8kHz/384kHz PCM input stream use one single data line
1: 352.8kHz/384kHz PCM input stream use two data lines

5.5 Software Revision Register

Register address: 0x06

	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Bit name	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
Access type	R	R	R	R	R	R	R	R
Default value	-	-	-	-	-	-	-	-

REV 7..4 Major revision
REV 3..0 Minor revision

5.6 Product ID Register

Register address: 0x07

	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Bit name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Access type	R	R	R	R	R	R	R	R
Default value	0	0	0	0	0	1	0	0

ID 7..0 Product ID code
Permanently set to 0x05 for backward compatibility with Q5 Module

5.7 Product Sub-ID Register

Register address: 0x09

	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Bit name	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
Access type	R	R	R	R	R	R	R	R
Default value	0	0	0	0	1	0	0	0

SID 7..0 Product SUB-ID code
Permanently set to 0x0A for Q8 Module

6 Related products

6.1 Backward Compatibility

The Q8 Module offers similar functionality as the previous Edel Q5 Upsampler Module and has been designed with backward compatibility in mind. Therefor products using the Edel Q5 will work with the Q8 without requiring any redesign effort. Compatibility consideration between the Edel Q5 and the Q8 Modules are detailed here below:

- Identical housing and pin-out
- Identical functionality
- Similar electrical specifications
- Hardware mode control is identical
- Software mode control offers the same registers and adds more options
- The Q8 offers increased calculation power and enhanced processing algorithms for better sound quality

6.2 Custom applications

The Q8 Module is based on a modern digital platform which runs engineered's software framework for digital audio processing. This core system can be used for many custom applications where specific processing is required:

- Cross-over
- Time/phase correction
- Equalization
- Compensation for loudspeaker characteristics
- Etc.

Please check our web site for more information and contact us for development of custom solutions that meets your product requirements.